Origins for Fermi Level Control in Metal/High-k/Si Stacks with Inserted Dielectric Layers

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Ultrathin dielectric capping layers are a prominent route for tuning band offsets and threshold voltages of advanced devices. Recent results obtained for several materials systems are presented and discussed. Ta_2O_5 is shown to be able to suppress the known dipole at Al_2O_3-SiO_2 interfaces. In a different system, the diffusion of Al inside an Al_2O_3-capped HfO_2-based device is studied in detail. The effect of the high temperature diffusion of Al to the HfO_2-SiO_2 interface is demonstrated, and presence of Al at that interface is correlated with the expected band offsets. La_2O_3 deposited in a similar way is known to have an opposite electrostatic effect. We show that La has a fundamentally different diffusion behavior under high temperatures, and that unlike Al it does not stop at the HfO_2-SiO_2 interface, but rather penetrates deep into the SiO_2.

Introduction

Controlling the metal gate’s effective work function (EWF), or Fermi level position, is an important aspect of modern high-k/metal gate (HKMG) devices (1). The EWF has a crucial role in the electrical performance of metal oxide semiconductor (MOS) devices and circuits. The use of ultrathin dielectric layers, commonly referred to as capping layers, at the metal-dielectric interface has emerged as the prominent route for achieving this control. In this work we present some of our recent results on the materials-physical origins of these effects.

Ta_2O_5 Electrostatics

In an earlier work a dipole layer that was created by the formation of Ta-suboxide at Ta-Al_2O_3 interfaces was identified and studied (2). Inspired by these results, we studied the electrostatic behavior of ultrathin Ta_2O_5 layers in Al_2O_3 MOS capacitors. For this end, the position (X, measured from the metal) of a thin (2 nm) atomic layer deposited (ALD) Ta_2O_5 layer was varied inside an 8 nm ALD-Al_2O_3 layer that served as a dielectric in an MOS capacitor (inset of Fig. 1a). The sample preparation details and physical properties of Ta_2O_5 are reported in (3).

Capacitance-voltage analysis of this series of devices reveals the following trend in the flat band voltages (V_FB, which is proportional to the EWF): as long as the Ta_2O_5 layer is not in contact with the bottom SiO_2 (namely for X<8 nm), V_FB is independent of the position of the layer (Fig. 1a). The lack of position-dependence shows that no significant charges exist inside the Ta_2O_5 layer or at its interfaces with Al_2O_3. By contrast, when Ta_2O_5 is in contact with SiO_2...
(X=8 nm), the $V_{FB}$ is reduced by 1±0.2 V. It has been shown in a control experiment that the contact between Ta$_2$O$_5$ and SiO$_2$ does not have any significant effect on $V_{FB}$ (Fig. 1b). In addition, a contact between SiO$_2$ and Al$_2$O$_3$ is known to increase the $V_{FB}$ and EWF (2, 4). It is therefore concluded from our results that Ta$_2$O$_5$ can inhibit this effect. The high permittivity (~22) of this material enables its scalable use as another degree of EWF control in devices such as NVMs (5) and others. Furthermore, Ta$_2$O$_5$ has recently been reported as a potential capping layer for reducing the interfacial SiO$_x$ at the Si-HfO$_2$ interface (6), thus its position in the device can offer another possible route for EWF control.

![Figure 1.](image1.png)

Figure 1. (a) The dependence of the flat band voltage ($V_{FB}$) on the distance of the Ta$_2$O$_5$ layer from the metal gate (X). Inset shows a schematic cross section of the MOS structures. (b) Capacitance-voltage curves of control samples showing no significant effect of the Ta$_2$O$_5$-SiO$_2$ interface on the $V_{FB}$, when no Al$_2$O$_3$ is involved. The decrease in capacitance is the result of the added Ta$_2$O$_5$ layer, yielding a dielectric constant of ~22.

**Al$_2$O$_3$ Capping for HfO$_2$ Devices**

HfO$_2$ is a more technologically relevant high-k dielectric and it is implemented in commercial devices since the first generation of HKMGs. Controlling the EWF in Hf-based devices can be done by the application of a capping layer at the metal dielectric interface. Rare-earth (RE) oxides, and most commonly La oxide, were shown to decrease the EWF of devices (7) while Al oxide was shown to increase it (8). The theoretical explanations for these effects are based on the assumption that the cap’s atoms diffuse through the high-k and reach its bottom interface with SiO$_2$ (9-12). Such diffusion was indeed shown for La by various techniques (13, 14) but the case of Al$_2$O$_3$ is significantly less studied.

In order to better understand the diffusion of Al in HfO$_2$-based MOS devices during a typical high temperature anneal, a series of capacitors was fabricated with a varying position of a thin (2 nm) layer of ALD-Al$_2$O$_3$. The Al$_2$O$_3$ layer was positioned at the top and bottom interfaces of the HfO$_2$ and in the middle of it, Fig. 2a. These samples were subjected to high and low temperature anneals (1000°C, 5 s and 400°C, 30 min, respectively) (15).

Examination of the flat band voltages reveals several trends (Fig. 2b). In the low temperature regime the “bottom” configuration displays a higher $V_{FB}$ compared to the other samples. This
increase of ~0.4V is consistent with the band alignment at the $\text{Al}_2\text{O}_3$-$\text{SiO}_2$ contact previously reported by us (2). More interestingly, in the high temperature regime, all the samples containing $\text{Al}_2\text{O}_3$ have a higher $V_{\text{FB}}$ compared to the “HfO$_2$-only” reference sample. Moreover, it can be seen in Fig. 2b that the closer the initial position of the $\text{Al}_2\text{O}_3$ layer to the $\text{SiO}_2$, the higher is the $V_{\text{FB}}$ increase. Altogether, these two electrical observations suggest a diffusion of Al from the $\text{Al}_2\text{O}_3$ layer to the bottom of the HfO$_2$ during a high temperature anneal.

Figure 2. (a) Schematic cross section of various positions of $\text{Al}_2\text{O}_3$ inside HfO$_2$ MOS capacitors. (b) Summary of the flat band voltages ($V_{\text{FB}}$) of all samples after low and high temperature anneals.

In order to evaluate this indirect observation, we combined transmission electron microscopy (TEM, FEI Titan operated at 300KV) and time-of-flight secondary ion mass spectrometry (ToF-SIMS, ION-TOF TOF.SIMS 5) to study the low and high temperature versions of the “middle” configuration. A comparison of Figs. 3a and 3c demonstrates that the layers remain uniform and continuous after the high temperature anneal (also evident from lower magnification images, not shown). It can further be seen that a new layer is formed at the Pt-HfO$_2$ interface after the high temperature anneal (Fig. 3c), with a corresponding shift in the concentration profiles (Fig. 3b and vertical lines). It should be noted that Pt was deposited after the high temperature anneal.

The key finding in Fig. 3 is the diffusion of Al from the middle of the stack to the bottom HfO$_2$-$\text{SiO}_2$ interface, and the accumulation of Al at that interface (emphasized by the shaded region of Fig. 3b). This confirms the indirect evidence that the diffusion of Al to the bottom interface is responsible to the increase in $V_{\text{FB}}$. By this we directly correlate between the electrical behavior (Fig. 2) and the presence of Al at the $\text{SiO}_2$ interface. Moreover, it is concluded that the initial position of the $\text{Al}_2\text{O}_3$, as well as Al-doping of the HfO$_2$ layer, can be used to fine-tune the EWF increase effect.
Comparison between Al$_2$O$_3$ and La$_2$O$_3$ Capping Layers

Several theoretical approaches were attempted to explain the opposite directions of the EWF shift caused by doping with La and Al [e.g. refs. (9-11)]. These theoretical works assume the same position of the dopant atom (Al or La), at the HfO$_2$-SiO$_2$ interface. However, we have shown that Al exhibits a different diffusion behavior compared to what was previously published on La. Considering this, it is of interest to compare the diffusion of La and Al under the same experimental conditions.

An 8 nm HfO$_2$ layer was ALD-grown on a 7 nm layer of thermal SiO$_2$. Nominally 2 nm thick layers of Al$_2$O$_3$ or La$_2$O$_3$ were grown on top of the HfO$_2$ layer by ALD (15) and by sputtering (La$_2$O$_3$ target, 3:10 O$_2$:Ar at ~9 mTorr), respectively. An annealing scheme similar to that described in the previous section was performed with the high temperature samples undergoing a spike anneal (1050°C, 5 s, N$_2$ atmosphere) and both the low and high temperature samples undergoing a low temperature anneal (400°C, 30 min, <10$^{-7}$ Torr).

The ToF-SIMS profiles of the Al$_2$O$_3$ cap (Fig. 4a) show a behavior that is quite consistent with the results described in the previous section. The accumulation of Al at the HfO$_2$-SiO$_2$ interface is clearly evident, in agreement with the finding of Fig. 3b, as well as the out-diffusion of Si to the free surface.

A distinctly different behavior is observed for the La$_2$O$_3$-capped sample (Fig 4b). First, it is noted that La signal is acquired from the HfO$_2$ layer that is positioned below it, even at low temperatures. A comparison to an un-annealed sample (not shown here) shows that this distribution is not the result of knock-in damage occurring during the sputtering process of the SIMS measurement. This means that unlike Al, even at 400°C La diffuses in HfO$_2$. This La diffusion profile, including the low temperature distribution, is consistent with previous works (13).
Unlike the case of Al, following the high temperature anneal the diffusion of La clearly doesn’t stop at the HfO$_2$-SiO$_2$ interface, but rather La is incorporated deep inside the bottom SiO$_2$ layer. Lanthanum’s tendency to react with SiO$_2$ has been observed much earlier (16), and has recently been thoroughly investigated by Essa and coworkers (13) alongside its diffusion in HfO$_2$.

Bosman and co-workers (17) have noted a slight (~0.6 nm) difference between the distributions of Al and La in annealed devices. However, the fact that they analyzed an extremely thin stack (~4 nm between the gate and Si) prevented them from finding a fundamental difference in the diffusion behavior of LaO$_x$ vs. AlO$_x$. Our intentional use of a thick, 7 nm bottom SiO$_2$, combined with the excellent depth resolution of ToF-SIMS, allow the unique observation that Al stops on SiO$_2$ while La diffuses through the SiO$_2$.

These observations affirm the position of Al at the HfO$_2$-SiO$_2$ interface, thus corresponding to the theoretical models mentioned above. However, our observations about the indiffusion of La through the SiO$_2$ imply that the electrostatic effect caused by La may originate at the SiO$_2$-Si interface and not where it was assumed thus far (the HfO$_2$-SiO$_2$ interface).

**Summary**

The material properties of thin dielectric capping layers and their effect on the electrical properties of MOS devices were studied in several material systems. In the case of Ta$_2$O$_5$, it was shown that a thin layer positioned at Al$_2$O$_3$-SiO$_2$ interfaces can suppress the dipole that is formed at these interfaces, adding a further degree of control over the Fermi level. With HfO$_2$ as a high-k dielectric, the diffusion of Al from Al$_2$O$_3$ capping layers was studied at the nanoscale. The presence of Al at the HfO$_2$-SiO$_2$ interface was correlated with an increase in the EWF. Finally, the diffusion behavior of Al and La from a top capping layer is compared under low and high temperature. It is shown that a fundamental difference exists between Al and La; Al is shown to stop diffusing and to accumulate at the HfO$_2$-SiO$_2$ interface whereas La is shown to diffuse inside- and be incorporated in the SiO$_2$ layer.
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References