Experimental evidence for the correlation between the weak inversion hump and near midgap states in dielectric/InGaAs interfaces

Igor Krylov,[1,a)] Lior Kornblum,[2] Arkady Gavrilov,[3] Dan Ritter,[1,3] and Moshe Eizenberg[1,2]
[1]*The Russell Berrie Nanotechnology Institute, Technion—Israel Institute of Technology, Haifa 32000, Israel*
[2]*Department of Materials Engineering, Technion—Israel Institute of Technology, Haifa 32000, Israel*
[3]*Department of Electrical Engineering, Technion—Israel Institute of Technology, Haifa 32000, Israel*

(Received 24 December 2011; accepted 4 April 2012; published online 24 April 2012)

Temperature dependent capacitance–voltage (C-V) and conductance-voltage (G-V) measurements were performed to obtain activation energies (E_A) for weak inversion C-V humps and parallel conductance peaks in Al_2O_3/InGaAs and Si_3N_4/InGaAs gate stacks. Values of 0.48 eV (slightly more than half of the band gap of the studied $In_{0.53}Ga_{0.47}As$) were obtained for E_A of both phenomena for both gate dielectrics studied. This indicates an universal InGaAs behavior and shows that both phenomena are due to generation-recombination of minority carriers through near midgap located interface states. The C-V hump correlates with the interface states density (D_{it}) and can be used as a characterization tool for dielectric/InGaAs systems. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4704925]

In order to continue the development of complementary metal oxide semiconductor (CMOS) devices, III-V layers such as InGaAs, due to their high electron mobility, are considered as alternative channel materials. The high density of states at the dielectric-semiconductor interfaces is one of the major challenges impeding the development of metal-insulator-semiconductor field effect transistors having III-V semiconductor channels. In general, and in particular in the case of an $In_{0.53}Ga_{0.47}As$ channel, it is widely believed that the interface states are generated by defects related to native oxides of the semiconductor.[1–4] A weak inversion capacitance-voltage (C-V) response, manifested by the appearance of a hump in this regime, is commonly observed in InGaAs based gate stacks; the exact physical origin of this hump is not fully clear.[5–9] Groeseneken and co-workers in their theoretical work attribute a weak inversion hump to carriers exchange between half of the band-gap located traps and both minority and majority carriers bands.[10] It is interesting to note that the weak inversion hump is located in the same voltage as the peak in parallel conductance, G_p, as a function of frequency measurements.[11] Nicollian and Brews attributed the parallel conductance peak in the weak inversion regime to generation—recombination processes through interface states.[11] We have recently observed that elimination of the weak inversion hump is accompanied with elimination of the parallel conductance peak in weak inversion voltages and with reduction in the interface states density.[12] Therefore, the origins of both phenomena, the weak inversion hump and the parallel conductance peak in the weak inversion region, should be the same. In the current work, we analyzed the temperature dependent C-V and G-V measurements using Arrhenius relationship in order to determinate the activation energies of the area of the weak inversion C-V hump and of the weak inversion parallel conductance peak for dielectric interfaces. C-V measurements were also carried out at various frequencies to study the frequency dependence of the weak inversion hump. Two different dielectrics (atomic layer deposited Al_2O_3 and plasma enhanced chemical vapor deposited Si_3N_4) were chosen to obtain universal trends and more basic understanding of the studied phenomena.

MOS capacitors were fabricated using an n-type Sn-doped $In_{0.53}Ga_{0.47}As$ layer ($5 \times 10^{16}\,cm^{-3}$) that was grown by metal-organic molecular beam epitaxy on an n-type InP substrate and capped by a 50 nm thick InP layer. Prior to dielectric deposition the InP capping layer was removed by HCl:H_3PO_4 solution. Si_3N_4 and Al_2O_3 were deposited separately on different $In_{0.53}Ga_{0.47}As$ samples within less than 5 min after capping layer removal. The Si_3N_4 layer was deposited without any pre-deposition treatment by plasma enhanced chemical vapor deposition (PECVD) using SiH_4 and NH_3 precursors in an N_2 ambient at a total process pressure of 900 mTorr at 250 °C. The Al_2O_3 was deposited by atomic layer deposition (ALD) using trimethylaluminium (TMA) and H_2O precursors at 300 °C. The thicknesses of the deposited Si_3N_4 and Al_2O_3 layers, measured by transmission electron microscopy, were 8 nm each. The gate metals, Ti/Au 1/200 nm thick, were deposited by electron beam evaporation using the lift-off technique for pattering. In order to eliminate defects induced by the metal deposition process,[13] all samples were annealed for 30 min at 400 °C in N_2.[14] C-V and G-V measurements were carried out in the dark using an impedance analyzer (HP 4284A) at the temperature range of 210–320 K and the frequency range of 5 kHz-1 MHz. The capacitance and conductance values were corrected for series resistance [using Eqs. (5.88), (5.9), and (5.91) in Ref. 11]. Cross-section high resolution transmission electron microscopy (HR-TEM) samples were prepared by focused ion beam (FIB) and imaged at 300 KeV (Titan 80–300, FEI).

Figures 1(a) and 1(b) represent typical Si_3N_4/InGaAs and Al_2O_3/InGaAs interfaces, respectively, following post-deposition anneal. Both micrographs reveal sharp InGaAs-dielectric interfaces without interfacial layers.

Figures 2(a) and 2(b) represent typical temperature and frequency dependent C-V hump behavior of the measured capacitors, when the increase in temperature and decrease in measurement frequency increase the C-V hump. The same

a)Electronic mail: krylov@tx.technion.ac.il.

 © 2012 American Institute of Physics

Downloaded 24 Apr 2012 to 132.68.209.77. Redistribution subject to AIP license or copyright; see http://apl.aip.org/about/rights_and_permissions

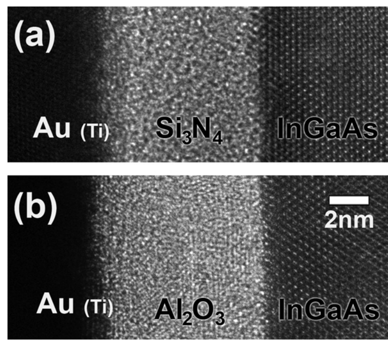

FIG. 1. Cross-sectional HR-TEM pictures of (a) $Au/Ti/Si_3N_4/In_{0.53}Ga_{0.47}As$ and (b) $Au/Ti/Al_2O_3/In_{0.53}Ga_{0.47}As$ gate stacks after post-deposition anneal.

trends were observed for the parallel conductance peak which is located in the same voltages as the C-V hump. Parallel conductance values for a given frequency were calculated using Eq. (5.77) in Ref. 11. In order to eliminate the influence of frequency dispersion in the accumulation region (~3% in the measured frequency range for both samples), the C-V data were normalized to match to the accumulation capacitance at 1 MHz, as shown in Figures 2(a) and 2(b). Figure 2(c) shows the C-V hump area (marked Q_{hump}), which has been chosen for hump characterization. To eliminate the influence of a frequency-dependent flatband shift on the Q_{hump} calculation, the C-V curves were horizontally aligned as marked on the abscisa of Fig. 2(c).

Figures 3(a) and 3(b) exhibit Arrhenius plots for Q_{hump} of both Si_3N_4/InGaAs and Al_2O_3/InGaAs samples for measurements at 10 kHz. The plots show two different regions for both samples—a low temperature region in which the C-V hump almost does not develop with T, and a high temperature region, in which there is an intensive increase of the hump; the transition between both regimes is located in the 240 K–250 K temperature range. The low temperature regime yields an activation energy of ~0.07 eV, and when the extrapolation of it is subtracted from the data of the high temperature regime, we obtain the curve with the blue squares (marked "corrected high-T region"), which yields an activation energy of ~0.48 eV. The value of activation energies (E_A) of the high temperature region is slightly higher than half of $In_{0.53}Ga_{0.47}As$ bandgap (the bandgap of $In_{0.53}Ga_{0.47}As$ is 0.74 eV) independent of the dielectric used. Therefore, Q_{hump} represents an inversion charge, which was generated through near-midgap located interface states.

Figure 4 shows Arrhenius plots of the parallel conductance peak height in the high temperature region for the Si_3N_4/InGaAs and Al_2O_3/InGaAs samples. Both samples yield the same activation energy, $E_A \sim 0.46$–0.47 eV, very close to the values obtained by the C-V hump analysis (Fig. 3). This indicates that both phenomena, the parallel conductance peak and the weak inversion hump, have the same origin—generation-recombination through near midgap located interface states, when the most effective interface states are located 0.1 eV below midgap. Therefore, Q_{hump} is related to minority carriers' charge, which was generated through interface states and was supplied to the inversion layer.

Figure 5(a) exhibits a linear behavior of Q_{hump}, normalized by insulator capacitance (C_{ox}), with 1/f for both Si_3N_4/InGaAs and Al_2O_3/InGaAs samples in the frequency range

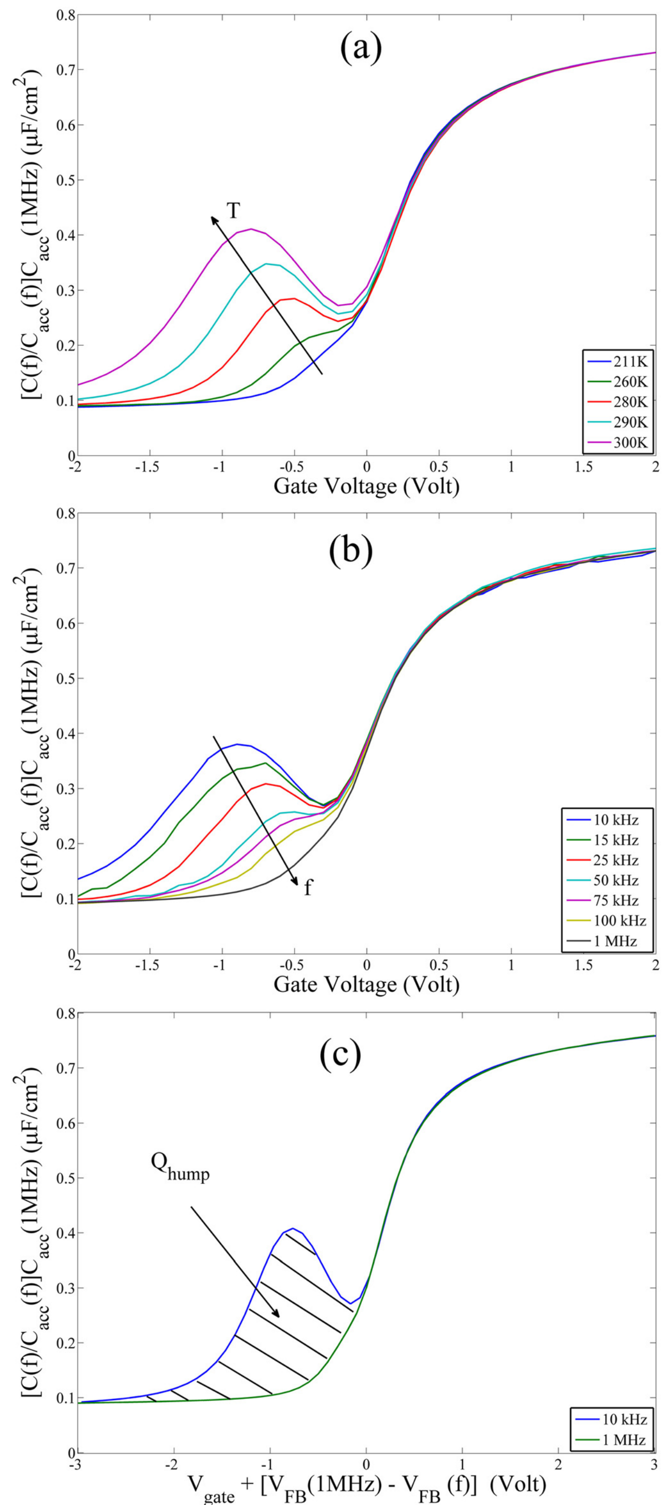

FIG. 2. Typical temperature (at 10 kHz) (a) and frequency (at 300 K) (b) dependent C-V characteristics of $Au/Ti/Al_2O_3/In_{0.53}Ga_{0.47}As$ gate stack, and C-V Q_{hump} determination (c).

of f = 10–100 kHz. The Si_3N_4/InGaAs gate stack shows lower normalized Q_{hump} values than Al_2O_3/InGaAs for the entire measured frequency range. It correlates with the lower near midgap D_{it} distribution extracted by Terman method in the Si_3N_4/InGaAs gate stack in comparison to the Al_2O_3/InGaAs gate stack (Fig. 5(b)). The results also correlates with our previous work where C-V hump elimination was accompanied with a significant D_{it} reduction.[12] Therefore,

Downloaded 24 Apr 2012 to 132.68.209.77. Redistribution subject to AIP license or copyright; see http://apl.aip.org/about/rights_and_permissions

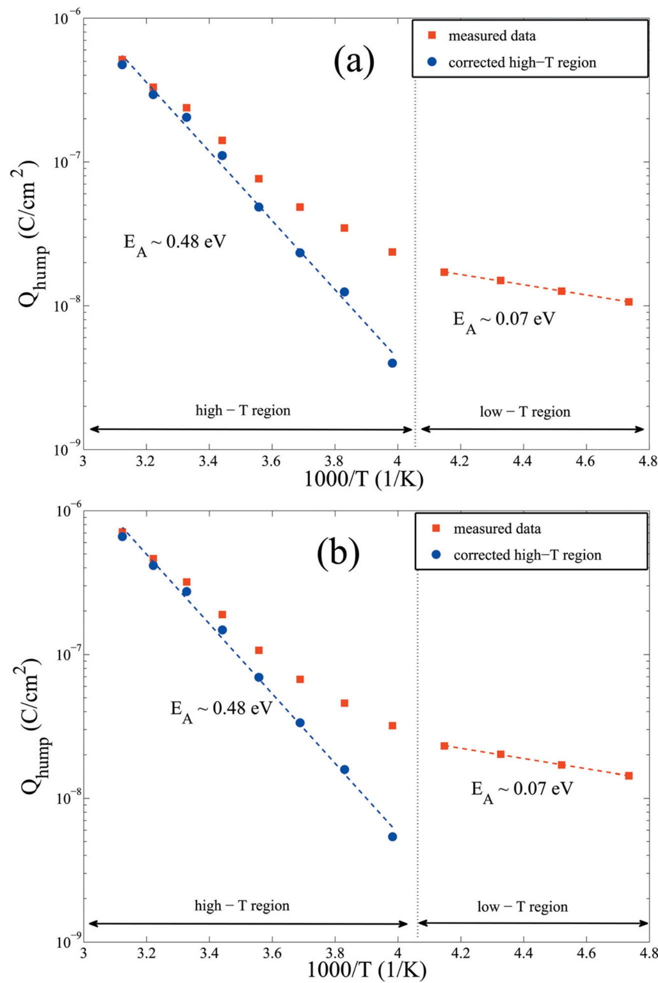

FIG. 3. Arrhenius plots of Q_{hump} plotted versus 1/T for Au/Ti/Si_3N_4/$In_{0.53}Ga_{0.47}As$ (a) and Au/Ti/Al_2O_3/$In_{0.53}Ga_{0.47}As$ (b) gate stacks at 10 kHz for the 210–320 K temperature range.

Q_{hump} at a given frequency, normalized by C_{ox}, can be used as an interface quality figure of merit. The observed lower D_{it} of Si_3N_4/InGaAs stacks in comparison with Al_2O_3/InGaAs stacks can be explained by better passivation ability of oxygen-free dielectrics compared to conventional oxygen-based dielectrics due to the suppression of InGaAs native oxides formation during dielectric deposition. In addition, the removal of InGaAs native oxides by the plasma during the PECVD process of Si_3N_4 cannot be ruled out.

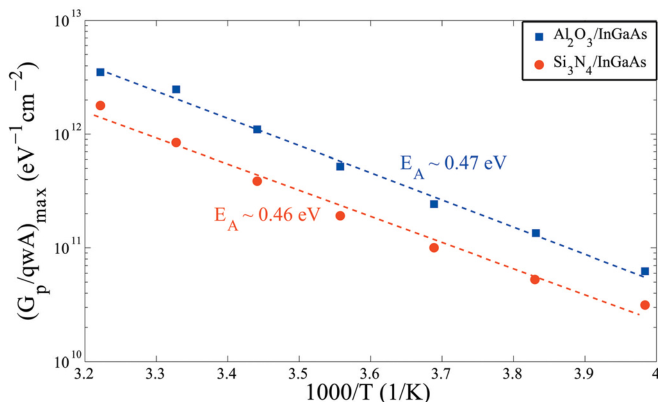

FIG. 4. Parallel conductance peak activation energy determination of Au/Ti/Si_3N_4/$In_{0.53}Ga_{0.47}As$ and Au/Ti/Al_2O_3/$In_{0.53}Ga_{0.47}As$ gate stacks at 10 kHz in the 210–310 K temperature range.

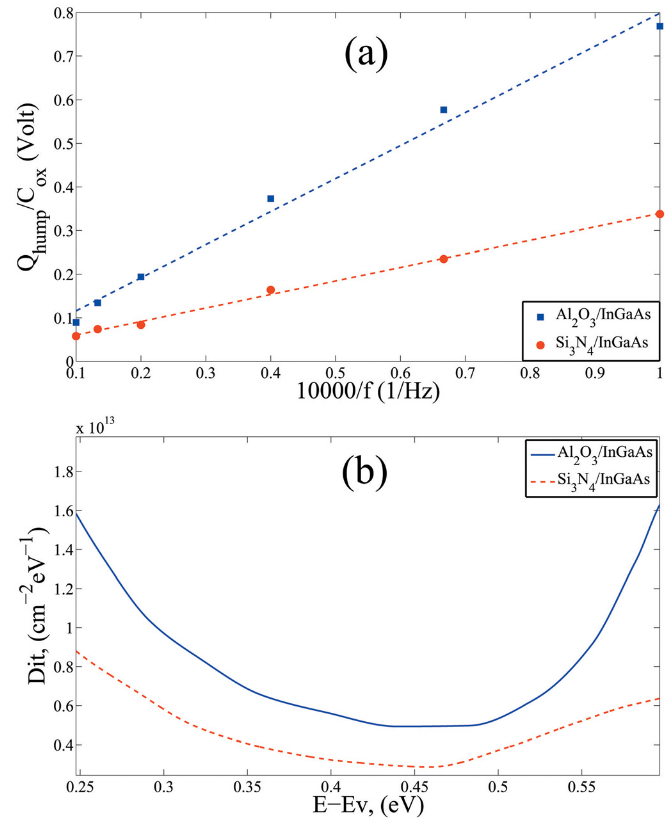

FIG. 5. Q_{hump}, normalized by C_{ox}, behavior in the 10–100 kHz frequency range (a) and D_{it} distribution extracted by Terman method (b) for Au/Ti/Si_3N_4/$In_{0.53}Ga_{0.47}As$ and Au/Ti/Al_2O_3/$In_{0.53}Ga_{0.47}As$ gate stacks at 300 K.

In summary, we showed that the weak inversion hump and the parallel conductance peak have the same activation energies without dependence on gate dielectric, indicating the same physical origin of both phenomena. The obtained activation energies were about 0.48 eV indicating that the origin of the both phenomenon is generation—recombination through interface states with the dominant role of interface states located 0.1 eV below midgap. An inverse proportional dependence of the weak inversion hump with the measurement frequency was also obtained.

The authors acknowledge the Russell Berrie Nanotechnology Institute (RBNI) at the Technion for financial support and Shimon Cohen and Sivan Fadida for technical support.

[1]S. Oktyabrsky and P. D. Ye, *Fundamentals of III-V Semiconductor MOSFETs* (Springer, New York, 2010).
[2]*Physics and Chemistry of III-V Compound Semiconductor Interfaces*, edited by C. W. Wilmsen (Plenum, New York, 1985).
[3]C. L. Hinkle, M. Milojevic, B. Brennan, A. M. Sonnet, F. S. Aguirre-Tostado, G. J. Hughes, E. M. Vogel, and R. M. Wallace, Appl. Phys. Lett. **94**, 162101 (2009).
[4]M. Huang, Y. Chang, C. Chang, Y. Lee, and P. Chang, Appl. Phys. Lett. **87**, 252104 (2005).
[5]E. J. Kim, L. Wang, P. M. Asbeck, K. C. Saraswat, and P. C. McIntyre, Appl. Phys. Lett. **96**, 012906 (2010).
[6]E. O'Connor, B. Brennan, V. Djara, K. Cherkaoui, S. Monaghan, S. B. Newcomb, R. Contreras, M. Milojevic, G. Hughes, M. E. Pemble, R. M. Wallace, and P. K. Hurley, J. Appl. Phys. **109**, 024101 (2011).
[7]R. Engel-Herbert, Y. Hwang, J. Cagnon, and S. Stemmer, Appl. Phys. Lett. **95**, 062908 (2009).
[8]Y. Hwang, R. Engel-Herbert, N. G. Rudawsli, and S. Stemmer, J. Appl. Phys. **108**, 034111 (2010).

Downloaded 24 Apr 2012 to 132.68.209.77. Redistribution subject to AIP license or copyright; see http://apl.aip.org/about/rights_and_permissions

[9]Y. Hwang, R. Engel-Herbert, and S. Stemmer, Appl. Phys. Lett. **98**, 052911 (2011).
[10]K. Martens, C. O. Chui, G. Brammerts, B. D. Jaeger, D. Kuzum, M. Meuris, M. M. Heyns, T. Krishnamohan, K. Saraswat, H. E. Maes, and G. Groeseneken, IEEE Trans. Electron Devices **55**(2) 547 (2008).
[11]E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology* (Wiley, New York, 1982), pp. 223–224.
[12]I. Krylov, A. Gavrilov, D. Ritter, and M. Eizenberg, Appl. Phys. Lett. **99**, 203504 (2011).
[13]G. J. Burek, Y. Hwang, V. Chobpattana, J. J. M. Law, W. J. Mitchell, B. Thibeault, S. Stemmer, and M. J. W. Rodwell, J. Vac. Sci. Technol. B **29**, 040603 (2011).
[14]I. Krylov, A. Gavrilov, S. Cohen, D. Ritter, and M. Eizenberg, “Physics and technology of high-k materials 9,” ECS Trans. **41**(3), 255–265 (2011).

Downloaded 24 Apr 2012 to 132.68.209.77. Redistribution subject to AIP license or copyright; see http://apl.aip.org/about/rights_and_permissions