Investigation of the band offsets caused by thin Al_2O_3 layers in HfO_2 based Si metal oxide semiconductor devices

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Ultrathin dielectric capping layers are a prominent route for threshold voltage control in advanced Si devices. In this work the position of an Al_2O_3 layer inside a HfO_2-based stack is systematically varied and investigated following a low and a high temperature anneal. Electrical results are compared with a sub-nanometer resolution materials characterization, showing a diffusion of Al to the bottom HfO_2 interface. A correlation is found between the presence of Al at the bottom interface and a flatband voltage increase. Based on these findings, we propose to use the position of the Al_2O_3 for fine-tuning the threshold voltage. © *2012 American Institute of Physics*. [doi:10.1063/1.3684939]

Controlling the threshold voltage is a significant challenge in the introduction of metal/high-k gate stacks in metal oxide semiconductor (MOS) technology.[1,2] Depositing ultrathin dielectric capping layers on top of the high-k dielectric emerged as a useful solution for controlling the effective work function (EWF) of the gate. By inserting a few monolayers of a different dielectric layer at the metal-dielectric interface, it is possible to tune the gate's EWF and thus tune the threshold voltage to the desired values.[2] Furthermore, this feature has recently been successfully implemented for reduction of the Schottky barrier height of contacts on Si (Ref. 3) and III-V semiconductors.[4]

Typically, atomic layer deposition (ALD) of ultrathin oxides of Al or La is used for increasing or decreasing the EWF, respectively.[5–7] Although capping layers are already implemented in modern devices, the physical origins of their role in affecting the band structure are not fully understood. Early works attributed the EWF shifts to the presence of atoms of the capping layers at the metal-dielectric interface.[8,9] On the other hand, a recent work[10] has shown experimentally that Al diffuses towards the HfO_2/SiO_2 interface; this was complemented by calculations showing that these atoms are more stable at this interface.[11–13] The electrostatic change induced by Al in the HfO_2/SiO_2 interface is attributed to various possible dipoles and dipoles screening.[12,14–16] Reference 12 provides further details on recent capping layers models.

In this work the electrostatic role of Al in HfO_2 is investigated using a series of samples with varying positions of an Al_2O_3 layer in HfO_2. While prior works in this subject included a ~1000 °C spike anneal similar to a technological process flow, in the present study the physics prior to this high temperature anneal is studied as well. A comparison of high and low temperature regimes enables to determine that in the low temperature regime Al affects the electrical properties only when it is in contact with the underlying SiO_2, while in the high temperature regime its effect is determined by the degree of Al diffusion in the dielectric stack.

A (100) Si wafer (p-type, $B \sim 5 \cdot 10^{17}\,cm^{-3}$) with a 5 nm layer of thermally grown SiO_2 was used as the substrate for all samples. The substrate was split and underwent different ALD sequences at 300 °C using tetrakis(dimethylamido)hafnium and water for HfO_2 deposition and trimethyl-aluminum and water for Al_2O_3 deposition. Half a sample of each configuration (specified in Fig. 1(a)) underwent a high-temperature rapid thermal anneal in an N_2 environment for 5 s at 1000 °C (will be denoted as a "high temperature" sample, while a "low temperature" sample refers to a sample that didn't undergo a 1000 °C aneal—only the 400 °C post metallization anneal mentioned below). Following this, metallization was done by e-beam evaporation of a 40 nm thick Pt layer through a shadow mask. Post metallization anneal was done in a vacuum furnace ($P < 10^{-7}$ Torr) on all samples for 30 min at 400 °C. Capacitance-voltage (C-V) measurements (HP 4284 A LCR meter) were carried out in a light sealed chamber at 100 KHz with the area of each capacitor measured using an optical microscope. Time of flight secondary ion mass spectrometry (ToF-SIMS, ION-TOF GmbH TOF.SIMS 5) depth profiles were taken in a dual mode using 25 KeV Bi_3^+ analysis ions and 0.5 KeV Cs^+ as the sputtering ions with a $81 \times 81\ \mu m^2$ acquisition area. Cross-section transmission electron microscope (TEM) samples were prepared by focused ion beam (FIB) and imaged at 300 KeV (Titan 80-300, FEI).

In order to systematically examine the effect of the Al_2O_3 position on the electrical behavior, four different sample configurations were fabricated, which are termed "top," "middle," "bottom," and "reference" schematically illustrated in Fig. 1(a).

The C-V curves of all the samples are presented in Fig. 1(b). All the samples other than the reference show less than 3% difference in the accumulation capacitance values, corresponding to about 8.9 nm of effective oxide thickness (or $0.39\ \mu F/cm^2$). The reference (HfO_2-only) samples show a slightly different accumulation capacitance due to the

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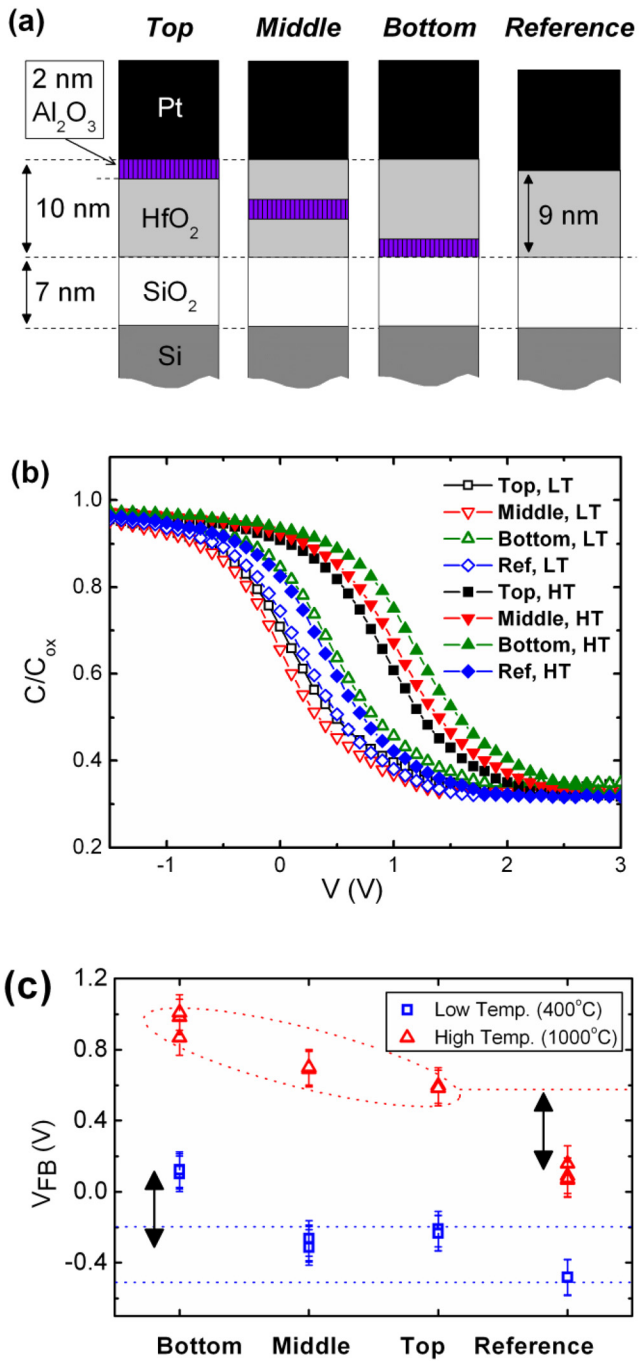

FIG. 1. (Color online) (a) Schematic view of the various samples, (b) C-V curves of low and high temperature samples and (c) summary of the flatband voltages

different dielectric stack (Fig. 1(a)). Therefore, in order to clearly illustrate the differences in V_{FB}, Fig. 1(b) is shown with a normalized capacitance ordinate.

In the low temperature regime the V_{FB} are distributed around -0.3 ± 0.15 V (dashed blue region in Fig. 1(c)), while the "bottom" sample has a V_{FB} value about 0.4 V higher. This shows that the Al_2O_3-SiO_2 contact is causing a band offset in the same direction and magnitude as previously reported.[17–20] This observation demonstrates that without a high temperature anneal Al_2O_3 capping layers not in contact with the bottom of the high-k dielectric have little or no effect on the band offsets.

Contrarily, Fig. 1(c) shows that in the high-temperature regime all the Al-containing samples feature V_{FB} values higher by $0.5 \div 0.9$ V with respect to the reference. Moreover, the closer the initial Al_2O_3 position to the SiO_2, the larger is the shift. In addition, the entire V_{FB} range is positively shifted following the high temperature anneal, which might be caused by changes in the fixed charges, HfO_2 crystallization and other reasons. The use of a reference with no Al_2O_3 enables the comparative analysis at both regimes.

Overall, the electrical results imply that Al diffusion towards the SiO_2 takes place at high temperatures, causing the observed V_{FB} shifts. To investigate the effect of the high temperature anneal on the depth distribution of Al, ToF-SIMS profiles were taken directly from the dielectric surface, from low and high temperature versions of the "middle" sample (Fig. 2(b)). The profiles were aligned next to cross-section TEM micrographs taken from low temperature (Fig. 2(a)) and high temperature (Fig. 2(c)) samples.

The ToF-SIMS results clearly show that Al diffuses and accumulates at the HfO_2-SiO_2 interface, as predicted by first principles.[11–13] This observation confirms the hypothesis, emphasized by a red filled region in Fig. 2(b), suggested by the electrical results and previous works that Al diffusion is responsible for the band offsets.

In addition, the appearance of lattice fringes in the HfO_2 regions in Fig. 2(c) suggests that this material crystallized, as expected,[21,22] during the high temperature anneal. Moreover, the profiles reveal out-diffusion of Al to the top free surface, and more surprisingly Si appears to out-diffuse and accumulate at the Al_2O_3 layer and at the top free surface. As emphasized by the vertical lines in Fig. 2, the TEM and ToF-SIMS results are consistently showing a $\sim$1 nm shift in the position of the HfO_2 stack towards the Si following the high temperature anneal. Due to its bright contrast, the layer at the Pt-HfO_2 interface (Fig. 2(c)) is likely composed mostly of Al and/or Si, also supported by the ToF-SIMS data. It can be suggested that the above mentioned shift is caused by a replacement of $\sim$1 nm of SiO_2 with the new layer. Further work is underway towards a better understanding of the nature and origin of this layer.

The correlation between the electrical properties and the composition changes (Figs. 1(c) and 2(b)) leads to the conclusion that inserted Al_2O_3 layers should not necessarily be "caps," namely on top of the high-k layer. Positioning the layer at the bottom or inside of the high-k layer can (a) provide a fine-tuning control over the EWF as seen by the high-temperature trend (Fig. 1(c)) and (b) implement a "bottom"-sample configuration for EWF or band-offset control for low temperature processes such as "gate last" and back-end metal-insulator-metal capacitors.[23] Moreover, the flexibility of ALD may enable EWF control using Al doping of the HfO_2, which is further useful as a glass former for increasing the crystallization temperature.[22]

How can the electrical results be explained by the observed composition and structure changes? Schematically, the initial bonding at the HfO_2-SiO_2 interface will be considered to be Hf-O-Si. Since the electronegativity of Al is halfway between that of Si and Hf, substituting any of these elements by Al would decrease the intrinsic dipole. This can be described as the addition of a reverse dipole, pointing from the SiO_2 to the HfO_2 which explains the EWF increase. As pointed out by Lin and Robertson,[12] a dopant inside

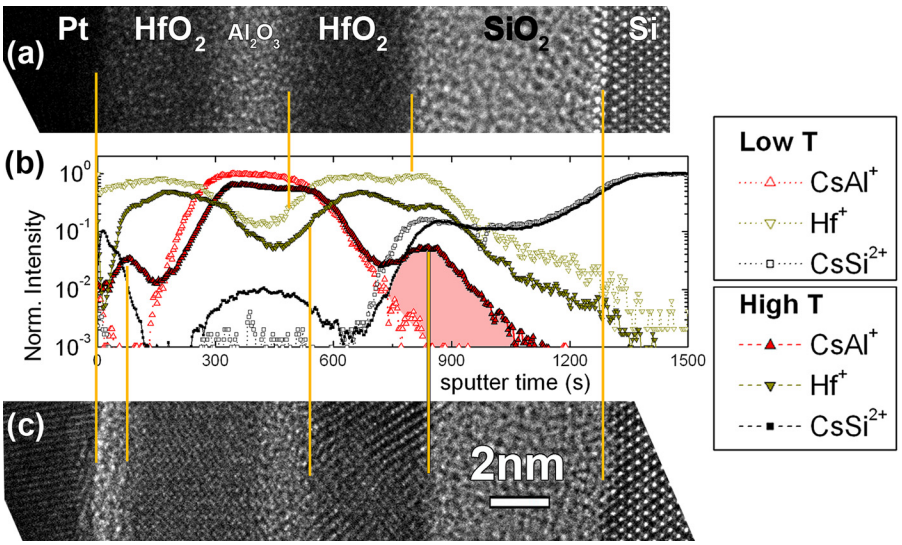

FIG. 2. (Color online) Cross sectional TEM micrographs were taken from sample "middle" (a) low temperature and (c) high temperature. (b) ToF-SIMS depth profiles comparing the low and high temperature regimes. Each of the three measured signals was normalized with respect to its maximum at the low temperature data.

either dielectric would create identical opposite dipoles with little macroscopic effect. Moreover, Hf substitution by Al is consistent with the results obtained with the low temperature "bottom" sample, representing a complete substitution of Hf. The higher shift observed at the high temperature regime can be attributed to a larger activation energy for the interfacial substitution of Al. This simplistic description cannot explain why La shifts the EWF in the opposite manner. The difference with respect to the La case will be discussed in detail in a future paper.

In summary, the position of an Al_2O_3 layer inside a HfO_2-based stack was systematically varied and compared at low and high process temperature regimes. Electrical results show V_{FB} increase when Al is in contact with the bottom SiO_2 in the low temperature regime. In the high temperature regime all the samples containing Al showed a V_{FB} increase. TEM and ToF-SIMS characterization have shown Al diffusion to the top and bottom HfO_2 interfaces in a representative sample where the Al_2O_3 is positioned at the middle of the HfO_2. Based on these findings, we propose using the position of the Al_2O_3 to fine-tune the threshold voltage.

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