Electronic transport of titanate heterostructures and their potential as channels on (001) Si

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Perovskite oxides and their heterostructures have demonstrated considerable potential for devices that require high carrier densities. These oxides are typically grown on ceramic substrates that suffer from low thermal conductivity, which limits performance under high currents, and from the limited size of substrates, which precludes large scale integration and processing. We address both of these hurdles by integrating oxide heterostructures with high carrier density 2D electron gases (2DEGs) directly on (001) Si. 2DEGs grown on Si show significant improvement of the high current performance over those grown on oxide substrates, a consequence of the higher thermal conductivity of the substrate. Hall analysis, transmission line measurements, and the conductance technique are employed for a detailed analysis of the carrier density, contact resistance, mobility, and electron drift velocities. Current densities of 10 A/cm are observed at room temperature with 2.9×10^{14} electrons/cm^2 at a drift velocity exceeding 3.5×10^5 cm/s. These results highlight the promise of oxide 2DEGs integration on Si as channels for high electron density devices. © 2015 AIP Publishing LLC. [http://dx.doi.org/10.1063/1.4930140]

The discovery of a two dimensional electron gas (2DEG) at the interface of two epitaxial oxides[1] has stimulated a decade of research effort into its physical properties, origins, and applications.[2–4] While research initially focused on the LaAlO$_3$-SrTiO$_3$ (LAO-STO) material system, similar 2DEGs have been discovered on STO when the LAO layer is replaced by oxides such as LaTiO$_3$,[5] NdTiO$_3$,[6] and NdAlO$_3$,[7] as well as amorphous[8,9] and epitaxial γ-Al$_2$O$_3$.[10,11] Among these examples, the rare-earth titanates (RTO) emerge as a prominent candidate with some of the highest reported carrier densities.[12,13] From the RTO family, GdTiO$_3$ (GTO) has been the most widely studied,[14] exhibiting a high electron density of $\sim 3.5 \times 10^{14}$ cm^{-2} (Ref. [12]) and ferromagnetism at low temperatures.[15] This density is an order of magnitude higher than that obtained with 2DEGs based on III–V semiconductors,[16–18] such as GaAs and GaN. Moreover, the titanates offer considerably higher breakdown fields and dielectric constants compared to III-Vs, making them possible candidates for electronic devices that are analogous to heterojunction field effect transistors[19] (HFET). Previous work has shown large charge modulation with high electron density devices,[20,21] which could benefit high current density electronics and plasmonic applications.

The majority of work on 2DEGs formed at oxide interfaces is based on heterostructures grown on ceramic oxide substrates, such as STO[1] or (LaAlO$_3$)$_{0.3}$(Sr$_2$AlTaO$_6$)$_{0.7}$ (LSAT).[12] Recently, we have demonstrated RTO-STO 2DEGs grown on Si wafers.[22,23] While the ceramic substrates are convenient for reasons of chemical stability, growing oxide 2DEGs directly on Si realizes several performance advantages. Integrating oxide 2DEGs on Si increases their potential for applications in integrated circuits and silicon-based technology. Furthermore, the growth of epitaxial oxides on Si is scalable,[24,25] whereas ceramic substrates are often limited by their small dimensions, which are typically ≤ 1 cm^2. Si further offers a considerably higher thermal conductivity of ~ 1.5 W·cm^{-1}·K^{-1}, a factor of 13–30 higher than the ceramics mentioned above. The superior thermal conductivity is expected to help reduce device heating while operating under high currents, which can induce thermal degradation of the mobility by Joule heating.

In this work, oxide 2DEGs are integrated onto silicon to evaluate their potential as electron channels for high carrier density devices. Transmission line measurements (TLM) and Hall measurements are used to study the transport properties, complemented by pulse measurements of the electron drift velocity in STO and its electric field dependence. High sheet carrier densities are observed at room temperature, and large current densities are obtained with considerably lower mobility degradation compared to previous work based on ceramic substrates. In addition, the use of a thicker top STO layer is found to result in a significant increase of the electron mobility. The physical origins of these electronic properties are discussed in terms of electron scattering by phonons, surfaces, and internal electric fields, and also the role of the Si substrate.

GTO-STO heterostructures are grown on high-resistivity (>3000 Ω cm) 2 in. (001) undoped float-zone Si wafers (Virginia Semiconductor) using a custom-built

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reactive molecular beam epitaxy (MBE) at a base pressure of $<5 \times 10^{-10}$ Torr. The growth is done by co-deposition at a background pressure of $\sim 5 \times 10^{-7}$ Torr of molecular oxygen and a substrate temperature of $600\,^{\circ}C$. Additional growth details have been described elsewhere.[22,23] The growth is monitored using reflection high-energy electron diffraction (RHEED) operated at 10 keV. The structure of the hetero-structures is analyzed with x-ray diffraction (XRD, Rigaku Smartlab) and tapping mode atomic force microscopy (AFM, Digital Instruments Nanoscope). Magnetotransport measurements are done with a Physical Properties Measurement System (Quantum Design) using the van der Pauw geometry. Contacting the heterostructure is done by Au sputtering on the corners of $\sim 5 \times 5$ mm^2 pieces that are scratched beforehand in order to contact all the layers of the heterostructure. Patterning for both TLM and drift velocity measurements is done using optical photolithography and Cl$_2$/BCl$_3$ based ICP-RIE plasma etching for mesa isolation. A Au/Ni/Al metal stack is used for ohmic contacts, and the samples are dipped in buffered hydrofluoric acid for 10 s just before metal deposition to reduce contact resistance.[20] Agilent B1500A and Diva D265 device analyzers are used for TLM and drift velocity measurements, respectively. Drift velocity measurements are done in pulsed mode (pulse width 500 ns and period 5 ms) to minimize heating effects.

This work describes the structure and electronic proper-ties of an epitaxial stack consisting of 50 unit cells (uc) of STO/10 uc GTO/4.5 uc STO/Si (001) (Fig. 1(c), inset). The electronic structure is compared to a structure with a thinner, 15 uc top STO layer, which is otherwise identical, described in recent work.[23] These structures are referred to as "thick" and "thin," respectively.

RHEED taken along the [100] direction of the top sur-face of the thick structure (Fig. 1(a)) shows sharp streaks on a low background, indicating a smooth crystalline surface. The surface roughness is quantified by tapping mode AFM (Fig. 1(b)), showing a root mean square roughness of 0.2 nm (0.5 uc) over the entire image. X-ray reflectivity (XRR) shown in Fig. 1(c) is fit (*GLOBALFIT 2.0*) with a low rough-ness of ~ 1 uc or less at all interfaces, and the fitted thick-nesses and the nominal thicknesses agree to better than 4% (Table I). The low roughness of 0.1 ± 0.1 nm obtained from XRR for the STO/Si interface highlights the effectiveness of the growth method in preserving the oxide/semiconductor interface quality, opening prospects for future functionalities by coupling of the oxide electronic structure with carriers in the semiconductor.

X-ray diffraction (XRD) curves of the (001) and (002) Bragg peaks (Fig. 2) show well defined finite thickness oscil-lations consistent with a high quality crystal with abrupt interfaces. These features, combined with the narrow rocking curve Fig. 2(c), indicate a high degree of crystalline order in the structure. The similarity of the lattice parameters of STO and GTO makes it hard to extract them independently from the fit; when the (pseudocubic) GTO out of plane lattice pa-rameter is constrained to be 3.921 Å,[15] the resulting out-of-plane parameter of STO is 3.911 ± 0.005 Å. The fit is based on the thickness values extracted from XRR (Table I). The small deviation from the bulk STO value of 3.905 Å can be
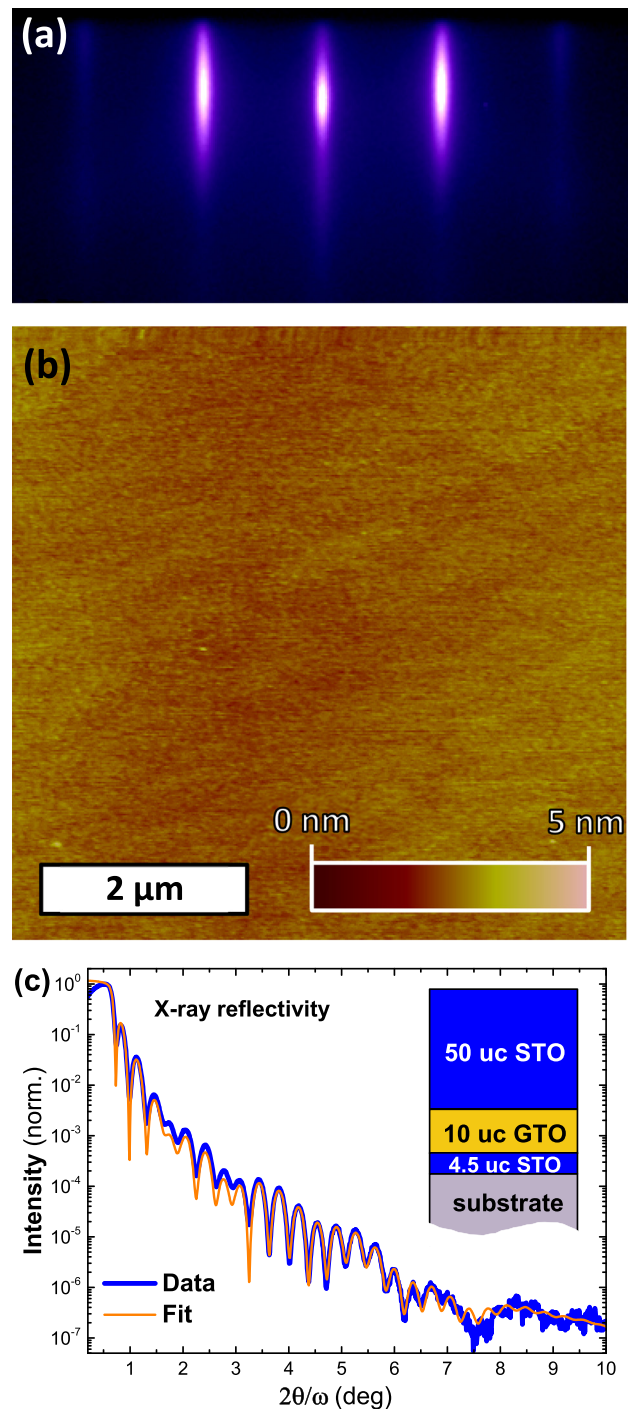

FIG. 1. Structural characteristics of the thick structure, with a top STO layer 50 uc thick. (a) RHEED pattern taken along the [100] direction from the top surface. (b) Contact mode AFM image. (c) X-ray reflectivity data and fit.

the result of a small residual thermal stress from the cooling step after growth, or a small deviation in the stoichiometry.[26] The presence of the pyrochlore phase[27] Gd$_2$Ti$_2$O$_7$ is ruled out by the absence of its major diffraction peaks in an XRD survey (PDF cards 00-054-0180 and 00-023-0259) and the absence of any non-perovskite reflections in the RHEED pat-tern during GTO growth.

The sheet resistance of the thick structure shows metal-lic behavior down to ~ 70 K (Fig. 3). In comparison, the thin structure, with an STO cap of 15 uc, shows a considerably

TABLE I. A comparison of the nominal layer thicknesses with the values extracted from XRR fitting (Fig. 1(c)). Nominal thicknesses are obtained by multiplying the nominal number of unit cells with the bulk lattice parameters of 3.905 Å and 3.921Å (Ref. 15) for STO and GTO, respectively. Errors are estimated from the fitting uncertainty.

Layer	Thickness, nominal (nm)	Thickness, measured ± 0.1 (nm)	Roughness ± 0.1 (nm)
STO	19.5	18.8	0.5
GTO	3.9	4.0	0.4
STO	1.8	1.8	0.3
Si			0.1

higher sheet resistance. This behavior is in agreement with the reports by Moetakef and co-workers,[12,15] which show a monotonic decrease in sheet resistance of a factor of 20 as the thickness is reduced from 20 nm to 5 nm.

The sheet carrier density and mobility are extracted from a combination of the longitudinal sheet resistance values and slope of the Hall measurements using $n_s = -1/(q \cdot R_H)$, where n_s is the sheet carrier density, q is the elementary charge, and R_H is the Hall coefficient derived from the slope of ρ_{xy} (transverse resistance) versus B curves. The values are summarized in Table II. The thick structure

exhibits a linear Hall behavior (ρ_{xy}-B, or a B-independent Hall coefficient) at all temperatures. In contrast, the behavior of the thin structure is highly non-linear at room temperature, and it becomes linear at low temperatures ($\sim$80 K). We attribute the non-linearity to the Hall response of carriers in the undoped Si substrate and its interface with STO.[23] When the contribution of the substrate to the conduction is similar to that of the 2DEG, non-linear behavior is observed. At low temperatures, as the substrate's intrinsic carriers freeze out, the 2DEG becomes the dominant contributor to the conduction and thus the carrier density can be extracted without multiple-parameter fitting. Since the thick sample is an order of magnitude more conductive, the contribution of the substrate's carriers becomes less significant, and the 2DEG electrons dominate the Hall signal.

Comparison of the sheet carrier density of the thick and thin structures at 80 K (Table II) reveals an increase of a factor of $\sim$2 in the carrier density of the thicker structure, showing a sheet density of 2.7×10^{14} cm^{-2} versus a value of 1.3×10^{14} cm^{-2} for the thin structure. In addition to increased carrier density, we also observe that the crystallinity is improved as the thickness is increased (Fig. 2(c)). We also note that the carrier density is less than that measured for GTO/STO interfaces grown on LSAT substrates with better
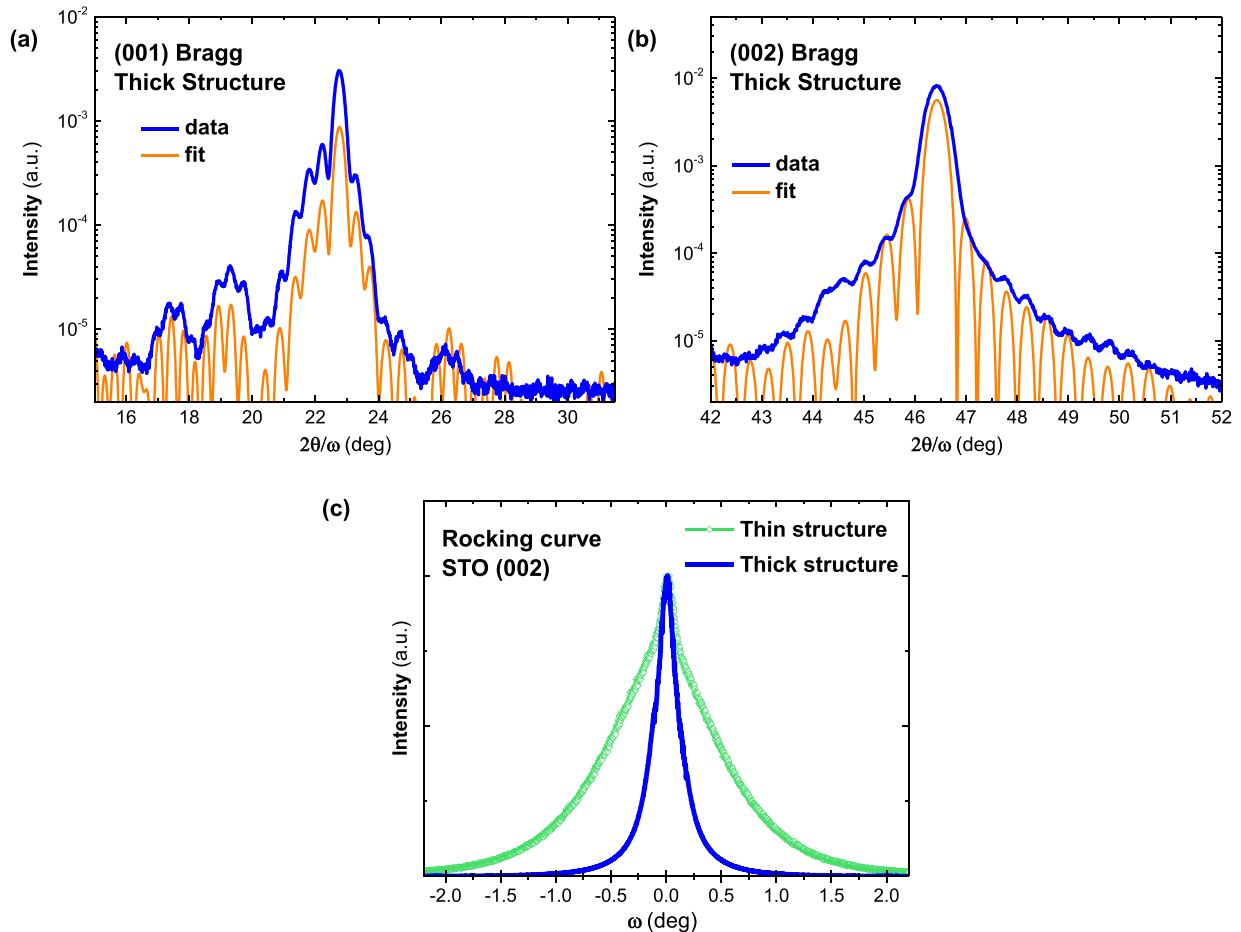

FIG. 2. X-ray structural characteristics of a GTO-STO heterostructure. (a) and (b) Bragg peaks of (001) and (002) reflections of the thick structure, respectively. Fitting parameters are obtained from the reflectivity analysis (Table I). The curves are scaled for clarity. (c) Rocking curves taken at the maximum of the (002) Bragg peaks, comparing the crystallinity of the thin and the thick structures (the rocking curves are normalized for clarity).
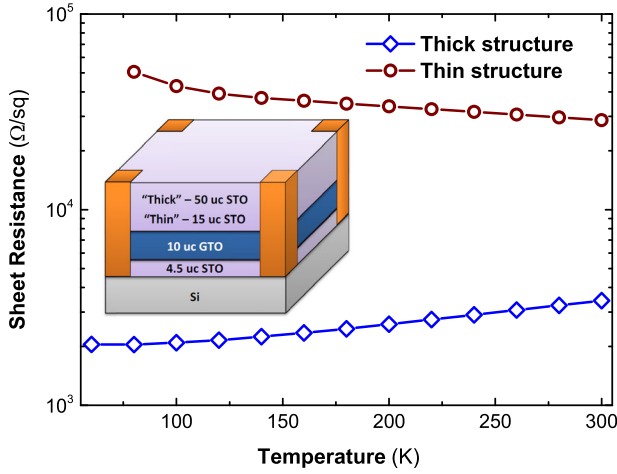
FIG. 3. 4-point electronic transport measurements, comparing the temperature dependence of the sheet resistance (R_S) of the thick and thin structures. Inset showing a highly simplified schematic of the measurement structure with Au at the corners.

crystallinity.[12,15] We speculate that structural defects may serve as electron traps, which decrease the observed free carrier density in films grown on silicon, and that increasing the thickness improves crystallinity and hence increases free carrier density. We note that for the thicker films, possible small variations of the O_2 growth pressure might lead to a slightly higher density of electronically active oxygen vacancies. We stress that the dominant factor in the decrease of the sheet resistance for the thick structure is an increase of the mobility, which increases from 0.9 to 11.4 cm^2 V^{-1} s^{-1} in the thicker structure at 80 K (Table II).

We attribute the lower mobility of the thin structure to surface (and interface) scattering, which becomes more dominant as the thickness of the STO layer approaches the electron mean free path.[28] The mean free path for 2DEGs in STO is estimated as ~10 nm (at 10 K),[5] which is about where the mobility is observed to decrease as the thickness is reduced (~19 nm to ~6 nm here and from 20 nm to 5 nm in Ref. 12). A similar trend was observed in (111) RTO-STO interfaces,[29] showing a continuous increase of mobility as the STO thickness increases from 5 nm to 30 nm. In addition, for thinner top STO layers, the electric field across the layers (in the out-of-plane direction, pointing from the bottom interface to the free surface) was shown to be larger,[20] further enhancing the effect of surface scattering. Summarizing, the thick sample exhibits a 2× increase in the carrier density at 80 K (Table II), which is mostly attributed to a lower

TABLE II. Comparison of the transport properties of the thick and thin structures. Values are extracted from Hall and sheet resistance data at temperatures where the Hall signal is linear with the magnetic field (ρ_{xy}-B curves).

	Thin structure, 80 K	Thick structure, 80 K	Thick structure, 300 K
Total sheet carrier density n_s (cm^{-2})	1.3×10^{14}	2.7×10^{14}	2.9×10^{14}
Mobility μ (cm^2 V^{-1} s^{-1})	0.9	11.4	6.2

concentration of structural defects in the thick structure (Fig. 2(c)), and about a 12× increase in mobility at this temperature, which is attributed to reduced surface scattering.

To assess the performance of the thick structure under high currents, it is important to ensure efficient charge injection at the contacts. The conduction band (CB) of STO is expected to be in the proximity of the CB of Si,[30,31] and therefore it is expected that a low work function (WF) metal would offer higher performance for the injection of currents into the oxides.[32,33] Here, we use Al as the contact metal for STO, with a WF that is lower by a few hundred meV compared to Cr,[34] which was used in Refs. 32 and 33. A 20 nm layer of Al is capped with 20 nm of Ni followed by 50 nm of Au. The metals are deposited at room temperature in a TLM[35] geometry having a systematically varying electrode spacing. The TLM measurements are performed at room temperature. Two point current-voltage (I-V) curves show a linear behavior, indicative of ohmic contacts (Fig. 4(a)). TLM yields the contact and sheet resistance from the two point resistivity values, using

$$R_{2pt} = 2R_C + \frac{L}{W}R_S, \quad (1)$$

where R_{2pt} is the 2-point resistance, R_C is the contact resistance, R_S is the sheet resistance, L is the spacing between contacts, and W is the contact width. Figure 4(b) presents a linear fit to R_{2pt} versus L, that yields a low contact resistance value of $R_C = 30 \pm 20$ mΩ cm, comparable to the 70 mΩ cm value previously reported.[21] The sheet resistance derived from the TLM measurements has a value of 3.40 ± 0.12 kΩ/□, in agreement with the 4-point measurement value at room temperature of 3.43 kΩ/□ (Fig. 3). The low contact resistance values demonstrate that current can be efficiently injected into the stack using contacts fabricated by simple materials and methods.

Current densities as high as 10 A/cm are observed for 2-point I-V measurements (Fig. 4(c)). More important, the currents do not saturate at these high densities, and they are limited by the compliance of the current source (fixed at 0.1 A, over a contact width of 100 μm, Fig. 4(c)). The I-V curve deviates from linear behavior at current densities exceeding ~4 A/cm, which is associated with thermal degradation of the mobility. The high current densities measured here show considerable improvement over previously reported transport characteristics for STO-based devices; for comparison, GTO-STO devices grown on ceramic substrates report currents as high as 1.0–1.2 A/cm,[19,20] and for STO devices as high as 0.02 A/cm,[36] 0.03 A/cm,[20] and 0.55 A/cm.[21]

In order to benchmark these high current densities, a relative mobility degradation is defined as the ratio between the measured current at a given field and the current calculated at this field by extrapolating the low-voltage I-V slope. This parameter represents the deviation of the I-V curve from ideal linear behavior, caused by mobility degradation, and it enables comparison of devices with different R_S and contact spacing (L) values. We calculate the relative mobility degradation based on data published on a metal-semiconductor field effect transistor[21] (MESFET) using a 160 nm-thick oxygen deficient STO channel on LSAT, and to a transistor
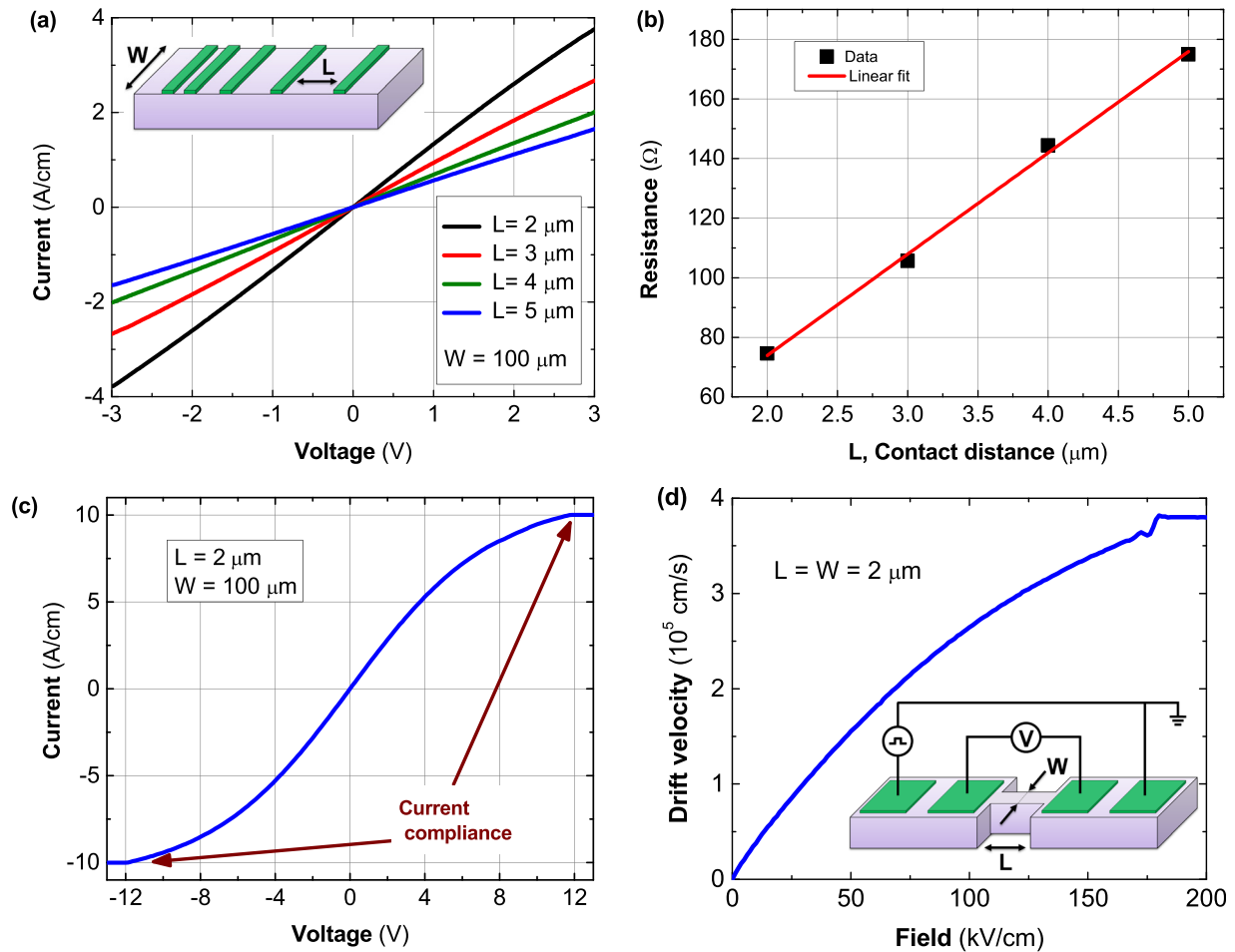
FIG. 4. High current transport through oxide 2DEGs. (a) Transmission line current-voltage measurements, with the inset showing a schematic view of the TLM test structure (not to scale). (b) Summary of the TLM measurements. (c) Extended current-voltage curve. (d) Drift velocity as a function of field using the conductance method,[37] with the inset showing a schematic of the measurement geometry.

fabricated from an STO/GTO/LSAT structure.[19] We compare the relative mobility degradation at a field of 14 kV/cm, which is close to the maximal voltages reported for these devices. At this field, the relative mobility degradation of the previous work is 36%–41%, versus less than 10% for the current results. To further illustrate this result, while previous work shows near-saturation at 14 kV/cm, for the geometry used here this field translates to 2.8 V, where Fig. 4(c) shows an almost linear behavior.

The saturated electron drift velocity, v_s, plays an important role in the power and frequency performance of devices.[38–40] The field-dependent electron drift velocity, v, is measured at room temperature using the conductance method,[37] with

$$v = \frac{I}{qwn_S}, \qquad (2)$$

where I is the current, q is the electron charge, w is the constricted width (Fig. 4(d), inset), and n_s is the sheet carrier density as extracted from the Hall data (Table II). Current pulses are injected through the outer contacts with a width of 500 μs and a period of 200 ms, to minimize heating, and the field is extracted from the voltage drop across the inner contacts. Drift velocities of $>3.5 \times 10^5$ cm/s are obtained using Eq. (2) (Fig. 4(d)). Similar to the current density, the drift

velocity does not saturate and is limited by the instrumental compliance. The low field mobility is calculated from the slope near the origin to be 4.5 cm^2 V^{-1} s^{-1}, which is slightly lower than the Hall mobility of 6.2 cm^2 V^{-1} s^{-1}. This drift velocity is an order of magnitude lower than the saturation velocities of common semiconductors,[41] such as Si, Ge, and GaAs, and is almost two orders of magnitude lower than that of nitride semiconductors[42] and SiC.[43] However, this advantage is compensated in the oxide 2DEGs in terms of conductivity by the considerably higher sheet carrier densities. The confinement of the electrons between two high-k oxides provides further potential benefit for field effect devices.

The mobility of STO near room temperature and down to ~200 K depends strongly on the temperature due to longitudinal optical (LO) phonons scattering[44,45] as follows: $\mu_{LO} \propto [\exp(\hbar\omega_{LO}/k_B T) - 1]$, where μ_{LO} is the mobility component related to LO phonons, $\hbar$ is the reduced Planck's constant, ω_{LO} is the phonon frequency, k_B is Boltzman's constant, and T is the absolute temperature. As a result, even small Joule heating during high current operation can lead to a large mobility reduction. Therefore, the superior thermal conductivity of Si over the ceramic substrates mitigates Joule heating and the subsequent thermal degradation of the mobility.

In summary, titanate heterostructures are fabricated and evaluated for high carrier density and high current applications. Sheet carrier densities of $2.9 \times 10^{14} \, \text{cm}^{-2}$ with a mobility of $6.2 \, \text{cm}^2 \, \text{V}^{-1} \, \text{s}^{-1}$ are measured at room temperature for a 50/10/4.5 uc stack of STO/GTO/STO epitaxially grown on an insulating Si substrate. When the thickness of the top STO layer is reduced (15 uc), the mobility (at 80 K) decreases by an order of magnitude, which is attributed to scattering of electrons by the top surface. 2-point and TLM measurements show ohmic behavior for Au/Ni/Al contacts with a low contact resistance of $30 \pm 20 \, \text{m}\Omega$ cm. We observe high current densities of $10 \, \text{A/cm}$ with high drift velocities ($> 3.5 \times 10^5 \, \text{cm/s}$) and exceptionally low mobility degradation for oxides, which we attribute to the superior thermal conductivity of the Si substrate. These results highlight the potential of silicon integration of oxide heterostructures for high electron density devices, which leverages the high carrier densities for high currents while mitigating limitations caused by mobility degradation.

[1]A. Ohtomo and H. Y. Hwang, Nature **427**(6973), 423–426 (2004).

[2]J. Mannhart and D. G. Schlom, Science **327**(5973), 1607–1611 (2010).

[3]P. Zubko, S. Gariglio, M. Gabay, P. Ghosez, and J.-M. Triscone, Annu. Rev. Condens. Matter Phys. **2**(1), 141–165 (2011).

[4]S. Stemmer and S. James Allen, Annu. Rev. Mater. Res. **44**(1), 151–171 (2014).

[5]S. S. A. Seo, W. S. Choi, H. N. Lee, L. Yu, K. W. Kim, C. Bernhard, and T. W. Noh, Phys. Rev. Lett. **99**(26), 266801 (2007).

[6]P. Xu, D. Phelan, J. Seok Jeong, K. Andre Mkhoyan, and B. Jalan, Appl. Phys. Lett. **104**(8), 082109 (2014).

[7]X. Xiang, L. Qiao, H. Y. Xiao, F. Gao, X. T. Zu, S. Li, and W. L. Zhou, Sci. Rep. **4**, 5477 (2014).

[8]S. W. Lee, Y. Liu, J. Heo, and R. G. Gordon, Nano Lett. **12**(9), 4775–4783 (2012).

[9]D. Fuchs, R. Schäfer, A. Sleem, R. Schneider, R. Thelen, and H. von Löhneysen, Appl. Phys. Lett. **105**(9), 092602 (2014).

[10]Y. Z. Chen, N. Bovet, F. Trier, D. V. Christensen, F. M. Qu, N. H. Andersen, T. Kasama, W. Zhang, R. Giraud, J. Dufouleur, T. S. Jespersen, J. R. Sun, A. Smith, J. Nygård, L. Lu, B. Büchner, B. G. Shen, S. Linderoth, and N. Pryds, Nat. Commun. **4**, 1371 (2013).

[11]Y. Z. Chen, N. Bovet, T. Kasama, W. W. Gao, S. Yazdi, C. Ma, N. Pryds, and S. Linderoth, Adv. Mater. **26**(9), 1462–1467 (2014).

[12]P. Moetakef, T. A. Cain, D. G. Ouellette, J. Y. Zhang, D. O. Klenov, A. Janotti, C. G. Van de Walle, S. Rajan, S. J. Allen, and S. Stemmer, Appl. Phys. Lett. **99**(23), 232116 (2011).

[13]A. Janotti, L. Bjaalie, L. Gordon, and C. G. Van de Walle, Phys. Rev. B **86**(24), 241108 (2012).

[14]S. Stemmer, P. Moetakef, T. Cain, C. Jackson, D. Ouellette, J. R. Williams, D. Goldhaber-Gordon, L. Balents, and S. J. Allen, Proc. SPIE **8626**, 86260F (2013).

[15]P. Moetakef, J. Y. Zhang, A. Kozhanov, B. Jalan, R. Seshadri, S. J. Allen, and S. Stemmer, Appl. Phys. Lett. **98**(11), 112110 (2011).

[16]O. Ambacher, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, W. J. Schaff, L. F. Eastman, R. Dimitrov, L. Wittmer, M. Stutzmann, W. Rieger, and J. Hilsenbeck, J. Appl. Phys. **85**(6), 3222–3233 (1999).

[17]V. Umansky, M. Heiblum, Y. Levinson, J. Smet, J. Nübler, and M. Dolev, J. Cryst. Growth **311**(7), 1658–1661 (2009).

[18]L. Shen, S. Heikman, B. Moran, R. Coffie, N. Q. Zhang, D. Buttari, I. P. Smorchkova, S. Keller, S. P. DenBaars, and U. K. Mishra, IEEE Electron Device Lett. **22**(10), 457–459 (2001).

[19]M. Boucherit, O. F. Shoron, T. A. Cain, C. A. Jackson, S. Stemmer, and S. Rajan, Appl. Phys. Lett. **102**(24), 242909 (2013).

[20]M. Boucherit, O. Shoron, C. A. Jackson, T. A. Cain, M. L. C. Buffon, C. Polchinski, S. Stemmer, and S. Rajan, Appl. Phys. Lett. **104**(18), 182904 (2014).

[21]A. Verma, S. Raghavan, S. Stemmer, and D. Jena, Appl. Phys. Lett. **105**(11), 113512 (2014).

[22]E. N. Jin, L. Kornblum, D. P. Kumah, K. Zou, C. C. Broadbridge, J. H. Ngai, C. H. Ahn, and F. J. Walker, APL Mater. **2**(11), 116109 (2014).

[23]L. Kornblum, E. N. Jin, D. P. Kumah, A. T. Ernst, C. C. Broadbridge, C. H. Ahn, and F. J. Walker, Appl. Phys. Lett. **106**(20), 201602 (2015).

[24]X. Gu, D. Lubyshev, J. Batzel, J. M. Fastenau, W. K. Liu, R. Pelzel, J. F. Magana, Q. Ma, L. P. Wang, P. Zhang, and V. R. Rao, J. Vac. Sci. Technol., B **27**(3), 1195–1199 (2009).

[25]L. Zhang and R. Engel-Herbert, Phys. Status Solidi RRL **8**(11), 917–923 (2014).

[26]C. M. Brooks, L. F. Kourkoutis, T. Heeg, J. Schubert, D. A. Muller, and D. G. Schlom, Appl. Phys. Lett. **94**(16), 162905 (2009).

[27]P. Moetakef, D. G. Ouellette, J. Y. Zhang, T. A. Cain, S. J. Allen, and S. Stemmer, J. Cryst. Growth **355**(1), 166–170 (2012).

[28]H. Marom, J. Mullin, and M. Eizenberg, Phys. Rev. B **74**(4), 045411 (2006).

[29]S. Raghavan, J. Y. Zhang, and S. Stemmer, Appl. Phys. Lett. **106**(13), 132104 (2015).

[30]S. A. Chambers, Y. Liang, Z. Yu, R. Droopad, J. Ramdani, and K. Eisenbeiser, Appl. Phys. Lett. **77**(11), 1662–1664 (2000).

[31]F. Amy, A. S. Wan, A. Kahn, F. J. Walker, and R. A. McKee, J. Appl. Phys. **96**(3), 1635–1639 (2004).

[32]S. A. Chambers, M. Gu, P. V. Sushko, H. Yang, C. Wang, and N. D. Browning, Adv. Mater. **25**(29), 4001–4005 (2013).

[33]C. Capan, G. Y. Sun, M. E. Bowden, and S. A. Chambers, Appl. Phys. Lett. **100**(5), 052106 (2012).

[34]H. B. Michaelson, J. Appl. Phys. **48**(11), 4729–4733 (1977).

[35]G. K. Reeves and H. B. Harrison, IEEE Electron Device Lett. **3**(5), 111–113 (1982).

[36]Z. Zhengyong, L. Zhijiong, X. Jie, Z. Hengliang, and C. Shuai, IEEE Electron Device Lett. **34**(7), 927–929 (2013).

[37]I. A. Khan and J. A. Cooper, Jr., IEEE Trans. Electron Devices **47**(2), 269–273 (2000).

[38]E. Johnson, presented at the 1958 IRE International Convention Record, 1965; available at http://dx.doi.org/10.1109/IRECON.1965.1147520.

[39]R. W. Keyes, Proc. IEEE **60**(2), 225–225 (1972).

[40]W. v. Muench and E. Pettenpaul, J. Appl. Phys. **48**(11), 4823–4825 (1977).

[41]R. Quay, C. Moglestue, V. Palankovski, and S. Selberherr, Mater. Sci. Semicond. Process. **3**(1–2), 149–155 (2000).

[42]A. F. M. Anwar, W. Shangli, and R. T. Webster, IEEE Trans. Electron Devices **48**(3), 567–572 (2001).

[43]M. Roschke and F. Schwierz, IEEE Trans. Electron Devices **48**(7), 1442–1447 (2001).

[44]A. Verma, A. P. Kajdos, T. A. Cain, S. Stemmer, and D. Jena, Phys. Rev. Lett. **112**(21), 216601 (2014).

[45]E. Mikheev, B. Himmetoglu, A. P. Kajdos, P. Moetakef, T. A. Cain, C. G. Van de Walle, and S. Stemmer, Appl. Phys. Lett. **106**(6), 062102 (2015).