JOURNAL OF APPLIED PHYSICS **123**, 025302 (2018)

Oxide heterostructures for high density 2D electron gases on GaAs

Lior Kornblum,[1,2,a)] Joseph Faucher,[3] Mayra D. Morales-Acosta,[1] Minjoo L. Lee,[3,4] Charles H. Ahn,[1,5] and Frederick J. Walker[1]

[1]*Department of Applied Physics and Center for Research on Interface Structures and Phenomena (CRISP), Yale University, New Haven, Connecticut 06511, USA*
[2]*Andrew and Erna Viterbi Department of Electrical Engineering, Technion–Israel Institute of Technology, Haifa 32000, Israel*
[3]*Department of Electrical Engineering, Yale University, New Haven, Connecticut 06511, USA*
[4]*Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, Illinois 61801, USA*
[5]*Department of Mechanical Engineering and Materials Science, Yale University, New Haven, Connecticut 06511, USA*

(Received 13 September 2017; accepted 13 December 2017; published online 9 January 2018)

2D electron gases (2DEGs) that form at oxide interfaces provide a rich testbed of phenomena for condensed matter research, with emerging implementations in devices. Integrating such oxide systems with semiconductors advances these interesting phenomena toward technological applications. This approach further opens prospects of new functionalities arising from the potential to couple the 2DEG carriers with the semiconductor. In this work, we demonstrate the first integration of oxide 2DEGs with a direct bandgap III-V semiconductor. The growth and structural characteristics of (001) $GdTiO_3$-$SrTiO_3$ (GTO–STO) heterostructures on (001) GaAs are described. Analysis of the magnetotransport data yields a high electron density of $\sim 2 \times 10^{14}\,cm^{-2}$ per GTO–STO interface, and points to the oxide interface as the source of the carriers. The effect of structure and defects on the transport properties is discussed within the context of the growth conditions and their limitations. These results provide a route for integrating oxide 2DEGs and other functional oxides with GaAs toward future device prospects and integration schemes. *Published by AIP Publishing.* https://doi.org/10.1063/1.5004576

I. INTRODUCTION

The emergence of 2D electron gases (2DEGs) at the interface between two insulating oxides[1] has led to intensive research into their underlying physics and potential for applications.[2–5] Oxide 2DEGs have demonstrated the potential for a wide range of applications and devices,[6] such as field effect transistors,[7–10] spintronic devices,[11,12] charge modulation devices,[13] superconducting switches and devices,[14–16] resistive switching,[17] photodetectors,[18,19] sketched oxide devices,[20] and gas sensors.[19,21] Interfaces between rare-earth titanates and strontium titanate ($SrTiO_3$) provide an important material system exhibiting oxide 2DEG behavior.[22] A prominent member of this family is the $GdTiO_3$-$SrTiO_3$ (GTO–STO) interface, demonstrating exceptionally high electron densities, exceeding $3 \times 10^{14}\,cm^{-2}$ per interface.[23–25]

The realization of the full potential of oxide 2DEG devices in technology is limited by the use of single crystalline oxides as the substrate for their growth. The small dimensions of oxide substrates, typically below $1\,cm^2$, impose a limit on large scale fabrication. Integrating oxide 2DEGs with semiconductors provides the potential for overcoming these hurdles and bringing oxide functionalities closer toward technological applications.[26–30] Since the first demonstration of epitaxial growth of STO directly on Si,[31] scalable approaches have shown large area[32] (8 in. wafers) and high rate[33,34] growth schemes. In addition to advantages in scalability, growing functional oxides on semiconductors offers a potential for seamless integration with conventional circuits.

Motivated by these prospects, we recently demonstrated the integration of high electron density oxide 2DEGs directly on Si.[35–37] In this work, we demonstrate an approach for extending these capabilities to the III-V semiconductor family, using GaAs as a gateway. We present the growth, structure, and electronic transport of epitaxial GTO–STO heterostructures grown on GaAs wafers. The technological maturity of band-structure engineering in III-V semiconductors opens further prospects of coupling between the high electron density of the oxide 2DEGs and the semiconductor, with a potential for new functionalities.

II. EXPERIMENTAL

The concept above is implemented by the epitaxial growth of 200 nm unintentionally-doped (001) GaAs using molecular beam epitaxy (MBE, Veeco Gen II) on a 4 in. (001) semi-insulating GaAs wafer (AXT, $\rho > 10^8\,\Omega\cdot$cm). The GaAs substrates are outgassed at 650 °C (measured by pyrometry) for 30 min under As_2 overpressure. The substrate is then cooled to 600 °C for GaAs growth, performed at a rate of 0.6 μm/h and a V/III ratio of 15. During the post-growth cooling of the wafer, a ~100 nm layer of As is deposited as a protective cap to prevent contamination and oxidation of the GaAs surface,[38] allowing the wafer to be transported in air to an oxide MBE chamber.[39] Epitaxial (001) STO and GTO are grown in a custom made reactive MBE system by thermally evaporating 99.99% pure Sr, Gd (Sigma Aldrich), and Ti (Alfa Aesar) at a base pressure of

[a)]Author to whom correspondence should be addressed: liork@technion.ac.il

$\sim 5 \times 10^{-10}$ Torr and a background O_2 pressure of 2–5 $\times 10^{-7}$ Torr. O_2 is introduced into the chamber using a manual leak valve with a nozzle directed at the substrate. $12 \times 12\,mm^2$ pieces of the GaAs substrate are loaded and supported by a 2 in. Si wafer on the back, where the substrate temperature is measured using a thermocouple.

The growth of STO-GaAs begins with the desorption of the As cap by heating the sample in vacuum ($\sim 3 \times 10^{-8}$ Torr) to 450 °C for ∼2 min in the oxide MBE chamber. The desorption is monitored *in-situ* by the appearance of a reconstructed crystalline surface[40] in the reflectance high-energy electron diffraction (RHEED, 10 kV) pattern [Fig. 1(a)]. The As desorption is reported to occur at 400 °C,[41] suggesting that the actual wafer temperature measured by the thermocouple here is lower by ∼50 °C than the reading in the present case. Guided by the work of Droopad, Contreras-Guerrero *et al.*,[40,42] half a monolayer (ML) of Ti is deposited at a substrate temperature of 430 °C in vacuum. At the same temperature, 1 ML of STO is then deposited by co-evaporating Sr and Ti in an oxygen background pressure of $\sim 2 \times 10^{-7}$ Torr, followed by the evacuation of the oxygen and annealing at 620 °C. The substrate is cooled to 320 °C where 5 ML of STO is deposited at $\sim 5 \times 10^{-7}$ Torr of oxygen, which is the pressure used for all subsequent STO and GTO growth steps. The layer is annealed in vacuum at 650 °C (∼1 min) where crystallization is observed by RHEED, the first observation of crystalline STO in this growth flow. The substrate is cooled down to 550 °C for the growth of subsequent STO and GTO [Fig. 2(a)]. A total thickness of 10 and 20 unit cells (u.c., referring to crystalline layers, unlike ML) STO on GaAs are grown, followed by a vacuum anneal at 650 °C [∼1 min, Fig. 1(b)]. These two variants will be referred to as the thin and thick structures, respectively [Fig. 2(a)]. A 5 ML layer of GTO is deposited at a substrate temperature of 550 °C, and is then crystallized by another vacuum anneal at 665 °C [∼1 min, Fig. 1(c)]. The structure is capped with a 5 u.c. layer of STO grown at 550 °C, and the entire stack is annealed for ∼1 min at 650 °C in vacuum before being cooled down to room temperature [Fig. 1(d)]. A reference sample consisting of a 20 u.c. STO layer is grown on GaAs under the same conditions without GTO, including the 665 °C anneal.

Transport measurements are performed on $5 \times 5\,mm^2$ pieces in the van der Pauw geometry with sputtered Au contacts.[36] Hall measurements were conducted by sweeping the field at a ± 5 T range at a constant current, in the 2.5–10 μA range. X-ray diffraction (XRD) is done with a Rigaku Smartlab diffractometer using monochromatic Cu Kα radiation.

III. RESULTS AND DISCUSSION

XRD patterns acquired from thin and thick STO/GTO/STO/GaAs structures and an STO/GaAs reference [Fig. 2(a)] show the (002) Bragg peaks of the oxides surrounded by finite thickness oscillations [Fig. 2(b)]. No impurity peaks are observed in larger 2θ ranges (Fig. S1, supplementary material). The resulting out-of-plane lattice constants are 3.943(5) Å for the thin and thick structures and 3.953(7) Å for the reference sample. The XRD data for all samples are analyzed as a single STO layer, due to the difficulty of distinguishing the GTO contribution. This is the result of the similarity of the lattice constant of GTO[23,36] to STO and the relatively small amount of GTO in the structures.

The out-of-plane lattice parameters are larger than the nominal value of 3.905 Å for bulk STO. In the general case, this observation could be the consequence of compressive in-plane strain, which causes anisotropic distortions of the unit cell, or by cation stoichiometry deviations,[33,43,44] which result in an isotropic enlargement of the unit cell. The lattice mismatch between the 45°-in-plane-rotated oxide and GaAs is −2.3%, and thus, under the in-plane strain scenario, the oxide is expected to be under *tensile* strain. However, the oxides are more likely to be fully relaxed, considering the large lattice mismatch with the substrate. This expectation is verified by measurement of the (103) Bragg peak of the thin structure [Fig. 2(d)], yielding an in-plane lattice parameter of 3.94(1) Å, similar to that of the out-of-plane lattice parameter. Altogether, the XRD analysis indicates that the oxide layers are relaxed with respect to GaAs. Therefore, the increase in the lattice parameters with respect to the bulk is ascribed to off-stoichiometry, caused by a small deviation from the optimal Sr:Ti ratio. In comparison to similar GTO/

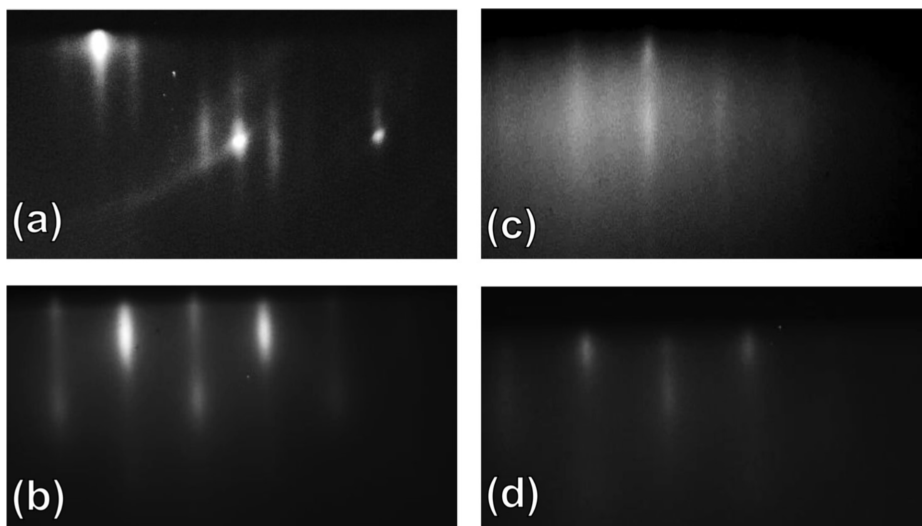

FIG. 1. RHEED images taken from (a) a clean GaAs surface after As-desorption, (b) after 20 u.c. of STO, (c) after 5 u.c. of GTO, and (d) after the last 5 u.c. of STO of the structure. Images are acquired along the [010] azimuth of each crystal surface.

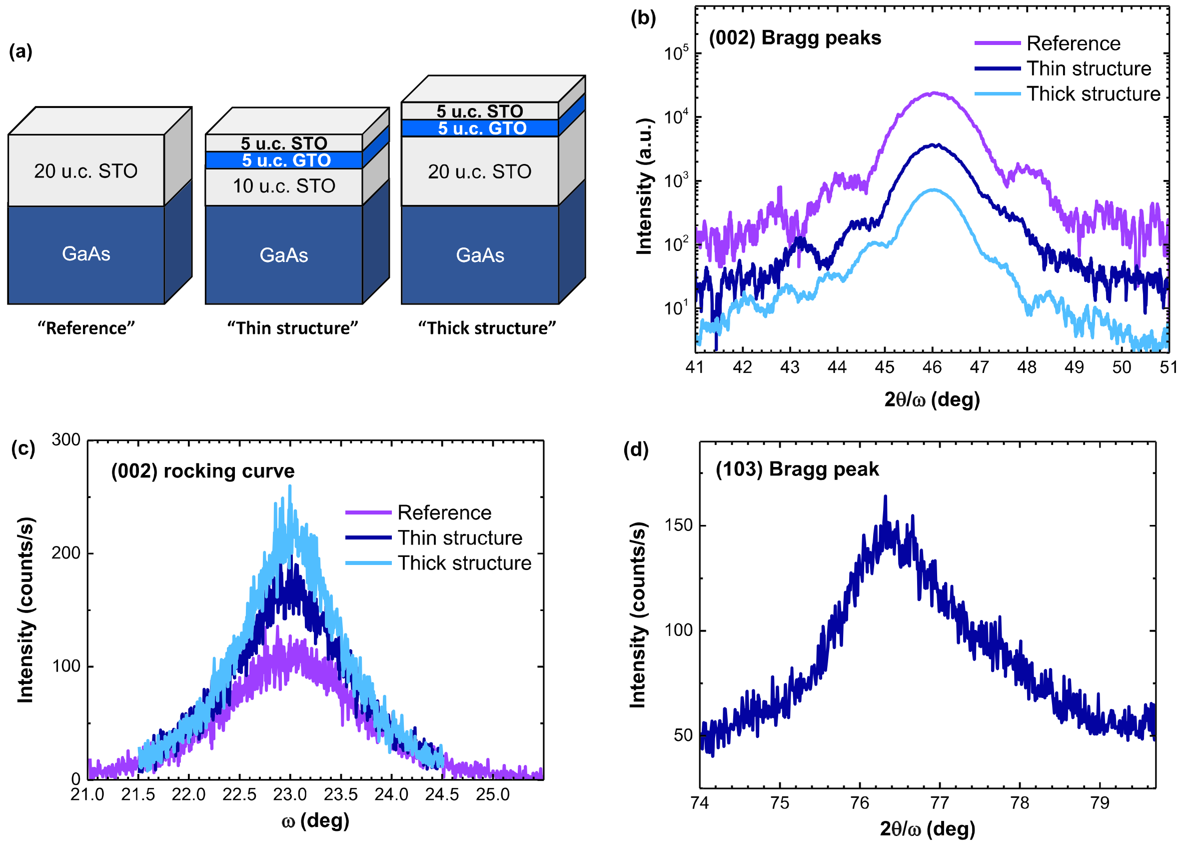

FIG. 2. Structures of the different samples. (a) Schematic cross-section of the various structures and their designations. (b) (002) Bragg peaks of the films with (c) corresponding rocking curves, (d) in-plane (103) peak acquired from the thin structure.

STO structures grown on Si,[36,37] the RHEED patterns (Fig. 1) and the rocking curves [Fig. 2(c)] show a slightly higher degree of disorder in the current case of GaAs. The higher crystallinity of the structures grown on Si is attributed to the smaller lattice mismatch (+1.7% on Si versus −2.3% on GaAs) and to the higher thermal stability of Si.

The temperature-dependent sheet resistance (R_S) of the heterostructures [Fig. 3(a)] shows considerable reduction in the R_S value for structures with GTO–STO interfaces, compared to the STO-only reference sample. Moreover, the sheet resistance of the GTO–STO structures does not depend on the STO thickness. The resistivity is found to be independent of the GTO thickness in previous work,[24,36] validating that the increased conductivity is a GTO–STO interface effect.[23] The sheet resistance of a bare GaAs substrate that underwent the same As desorption process exceeds the instrumentation limit, in the MΩ range. The sheet carrier density [Fig. 3(b)] is extracted from Hall measurements using $n_s = -1/(q \cdot R_H)$, where n_s is the sheet carrier density, q is the electron charge and R_H is the Hall coefficient, extracted from the linear slope of the Hall voltage versus magnetic field curves. The GTO–STO structures exhibit sheet electron densities of $6–7 \times 10^{14}\,cm^{-2}$ near room temperature, presenting an increase of about 3× over the STO reference with an electron sheet density of $2.5 \times 10^{14}\,cm^{-2}$. This observation is in agreement with the reduction in the sheet resistance when GTO is included in the stack [Fig. 3(a)]. Subtracting the STO-only carrier density from that of each GTO–STO structure, we obtain a sheet carrier density of $2 \pm 0.5 \times 10^{14}\,cm^{-2}$ per GTO–STO interface. This value is between $9 \times 10^{13}\,cm^{-2}$ observed for GTO–STO stacks on Si[36] and $3 \times 10^{14}\,cm^{-2}$ reported for such structures grown on single-crystal oxide substrates.[24]

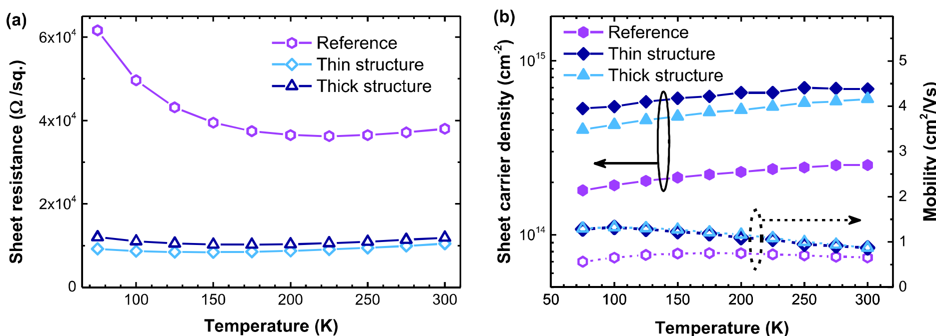

FIG. 3. Temperature dependence of the electronic transport of the structures; (a) 4-point sheet resistance, (b) sheet carrier density and electron mobility. The lines serve as a guide for the eye.

When similar structures are grown on Si, nonlinear Hall behavior (referring to transverse resistance, ρ_{xy}, versus magnetic field) is typically observed near room temperature.[35,36] The nonlinearity is attributed to intrinsic carriers in the semiconductor[37] operating as parallel conduction channels.[45] By contrast, in the present work, the Hall behavior is linear across the entire temperature range; we attribute this to the lower intrinsic carrier density in GaAs, which causes the high electron density in the oxide to dominate the Hall signal.

During growth, the oxygen partial pressure is limited in order to prevent oxidation of the semiconductor surface. Since oxygen vacancies act as electron donors in STO, both in the bulk[46] and at the interface,[47,48] we consider vacancies as the most likely source of the carriers observed in the STO-only reference. The short 650° and 665 °C vacuum anneal steps are likely to promote reduction of these oxides. These conditions feature a higher substrate temperature and a lower oxygen activity compared to the growth of these structures on Si, at 600 °C and 5×10^{-7} Torr O_2,[36] accounting for the higher electron densities observed here. Other explanations for the increase in the carrier density observed here versus structures grown on Si can be considered. A possible hypothesis is that the higher growth temperatures used here resulted in less defects, thus reducing compensation which could result in more carriers. However, this hypothesis is not in agreement with the broader rocking curves [Fig. 2(c)] compared to Si[37] that suggest the current samples have a larger defect concentration. Furthermore, this hypothesis does not explain the high carrier densities in the STO-only reference where vacancies are the only likely source of carriers. Alternatively, the higher temperature could promote ionic intermixing at the GTO–STO interface, which is another potential source of carriers.[49,50] While some interfacial intermixing is likely, in GTO–STO heterostructures that were grown at higher temperatures,[23,24] intermixing did not appear to play a significant role. Furthermore, since the STO-only reference exhibits $\sim 2 \times 10^{14}\,\mathrm{cm}^{-2}$ carriers [Fig. 3(b)], we consider oxygen vacancies are a likely source for the additional carriers.

The electron mobility values [Fig. 3(b)] are determined from the Hall data as $\sim 1\,\mathrm{cm}^2\,\mathrm{V}^{-1}\mathrm{s}^{-1}$, with the reference sample showing slightly lower values compared to the GTO–STO structures. The lower mobility of the latter is attributed to a slightly lower crystalline quality of the STO-only structure, as is evident by the rocking curve data in Fig. 2(c). We note that the ~25% lower mobility of the reference structure is not the main contributor to the ~3.5× higher resistivity of this sample [Fig. 3(a)]; rather, it is the higher carrier densities [Fig. 3(b)] originating at the GTO–STO interfaces (the magnitudes refer to room temperature; the trend is correct for all temperatures).

The increase in mobility at low temperatures is in qualitative agreement with previous work, but the extremely small range highlights the negligible effect of phonon scattering,[51] compared to temperature-independent impurity scattering. Altogether, these mobility values are comparable to similar structures grown on silicon[37] and are orders of magnitude lower than those reported for similar structures on oxide substrates[24] grown at temperatures of 800°–900 °C.[52] This behavior is attributed to a higher degree of structural defects, a consequence of the lower growth temperatures employed here (<665 °C) required for maintaining the interface stability with the semiconductor substrate. Compared to oxide substrates, the relatively higher defect densities observed with structures grown on semiconductors result in lower mobility values. These defects and disorder reduce the mobility through various possible scattering and localization mechanisms. Our results indicate that a better control of the oxide stoichiometry may improve the structural characteristics and thereby lead to higher mobility values. This provides a route for enhancing the electronic transport despite the limitations on the growth conditions imposed by the semiconductor substrates.

IV. CONCLUSIONS

We present a route for integrating high-carrier oxide 2DEGs with (001) GaAs using epitaxial growth of GTO–STO heterostructures. Structural analysis reveals an isotropic enlargement of the lattice parameter, which is attributed to an imperfect oxide stoichiometry. GTO–STO structures exhibit high electron densities of $2 \pm 0.5 \times 10^{14}\,\mathrm{cm}^{-2}$ per GTO–STO interface. This magnitude is determined after the removal of a contribution of $2 \pm 0.5 \times 10^{14}\,\mathrm{cm}^{-2}$ electrons found in the STO-only reference. The reference electron densities are ascribed to oxygen vacancies that form during growth. These results outline a route, and its limitations, for integrating oxides with high carrier densities on top of a direct bandgap III-V semiconductor.

SUPPLEMENTARY MATERIAL

See supplementary material for wide range XRD patterns of the three oxide structures.

ACKNOWLEDGMENTS

This work was funded with the support from the National Science Foundation through NSF DMR-1309868 and NSF MRSEC DMR-1119826. The authors thank Professor Emil Zolotoyabko for fruitful discussions and Timothy McHugh for technical assistance.

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