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Single Atomic Layer Ferroelectric on Silicon

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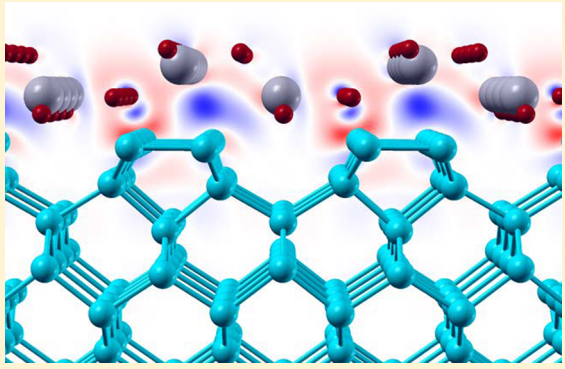
Supporting Information

ABSTRACT: A single atomic layer of ZrO_2 exhibits ferroelectric switching behavior when grown with an atomically abrupt interface on silicon. Hysteresis in capacitance−voltage measurements of a ZrO_2 gate stack demonstrate that a reversible polarization of the ZrO_2 interface structure couples to the carriers in the silicon. First-principles computations confirm the existence of multiple stable polarization states and the energy shift in the semiconductor electron states that result from switching between these states. This monolayer ferroelectric represents a new class of materials for achieving devices that transcend conventional complementary metal oxide semiconductor (CMOS) technology. Significantly, a single atomic layer ferroelectric allows for more aggressively scaled devices than bulk ferroelectrics, which currently need to be thicker than 5−10 nm to exhibit significant hysteretic behavior (Park, et al. *Adv. Mater.* 2015, *27*, 1811).



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A prominent challenge in semiconductor device physics involves the coupling of the reversible polarization of a thin film ferroelectric to mobile carriers in a semiconductor.[2,3] The idea is straightforward: a thin film ferroelectric layer is placed on top of silicon in a planar geometry, with the out-of-plane component of the nonvolatile ferroelectric polarization coupling electrostatically to the carriers in the silicon. Since the time this idea was patented in 1957 and explored in the early 1960s,[4,5] a number of approaches to realizing this invention have been pursued.[6−15] One simple approach is to deposit a conventional ferroelectric directly on top of silicon. While some success with this approach has been reported,[13,16−18] an ongoing challenge involves uncontrolled interface reactions that form a high density of interface traps or an insulating, nonferroelectric interface layer.[10,19] Interface traps screen the ferroelectric polarization from carriers in the silicon, reducing the switched modulation of transistor action. Moreover, depolarization of the ferroelectric may also arise from either a nonferroelectric insulator in the gate stack, such as SiO_2, or the presence of a potential drop across the semiconductor.[20,21] The depolarization fields that develop often exceed the coercive fields in conventional ferroelectrics, especially when the gate stack is scaled to nanometer dimensions.[10,17,22−27] For the 5 nm technology node, the required thickness of the ferroelectric layer is <2 nm. As the most promising candidates, recently discovered ferroelectric HfO_2-based thin films require a thickness of at least 5−10 nm to achieve a sizable hysteresis curve,[1,28−32] which creates a lower bound to the scale of potential HfO_2-based complementary metal oxide semiconductor (CMOS) devices. Recently, however, Lee et al. demonstrated the first ultrathin ferroelectric based on $HfZrO_x$ with a thickness of 1.5 nm.[33] Although the hysteresis is narrow, this study is an advancement towards the goal of achieving the next generation of MOS devices with zirconia/hafnia-based thin films.

Here, we introduce a new type of a ferroelectric, ZrO_2 on Si(001), that can be incorporated into a gate stack with a conventional dielectric such as amorphous Al_2O_3. One practical advantage is that this ferroelectric does not need to be epitaxial. At thicknesses on the order of a monolayer, the interface polarization of ZrO_2 is multistable and can be reversibly switched through the application of an electric field. A ferroelectric oxide at the ultimate thickness limit of a monolayer

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allows for aggressive scaling down of CMOS devices, as well as potentially enabling properties such as negative capacitance, which would reduce the required gate voltage and waste heat.[34−36]

The cubic form of ZrO_2 has the CaF_2 structure,[37] which can be stabilized through epitaxial growth on Si (001).[38,39] This structure is promising as a potential ferroelectric because cubic ZrO_2 grown on Si (001) is polar due to the separation between the positively charged Zr^{4+} plane and the negatively charged O^{2-} plane in the CaF_2 structure, which is often described as a rumpling of the neutral ZrO_2 planes. In bulk, the rumpling and polarization cannot be reversed or switched by the application of an electric field due to a large energy barrier and coercive field, resulting in a phase that is not ferroelectric. The approach we present here is to reduce the thickness to a single monolayer and thus reduce the energy barrier for switching, providing the ultimate length scale at the atomic level for the smallest devices. We test this idea theoretically and experimentally. First, we model a ZrO_2 monolayer on the surface of silicon. Our theoretical work predicts that a monolayer of ZrO_2 gives rise to a multistable interface structure that switches the silicon. We also realize this structure experimentally by growing a monolayer of ZrO_2 using physical vapor deposition and capping it with an amorphous Al_2O_3 (a-Al_2O_3) layer to complete the device gate stack.

The ability of a monolayer of ZrO_2 to exhibit a switchable polarization is studied with first-principles calculations performed using density functional theory (DFT) in a simulation cell consisting of a monolayer (ML) of ZrO_2 coherently strained to silicon. We find multiple configurations at low energy, with varying up and down polarizations. Two of these structures, shown in Figure 1a and b, are local minima, as shown in Figure 1c. Each minimum corresponds to one of the polarization states of the ferroelectric. The polarization is parametrized as δz, which is the difference between the average out-of plane position of the cations (Zr) and the anions (O). In the "up" and "down" configurations, δz is +0.04 Å and −0.06 Å, respectively. The difference in heights for the two polarizations is ∼0.1 Å, which is comparable to the ∼0.4 Å in ferroelectric tetragonal $BaTiO_3$.[40] The minimum energy transition path between these two states is computed via the nudged elastic bands (NEB) method with climbing images.[41] The transition occurs mainly by a shift of two Zr and three O atoms (in the 2 × 1 cell) in and out of the open channels on the Si surface that lie between dimmer rows along the 1× direction. The fourth O atom forms a bond with a Si dangling orbital and remains fixed through the transition. The energy barrier for homogeneous switching of the polarization states is 0.08 or 0.12 eV/ZrO_2 (depending on the direction of switching), which is larger than the barrier for a typical ferroelectric such as $BaTiO_3$, which has a DFT-calculated barrier of 0.02 eV/$BaTiO_3$.[42] We note that theory predicts a large barrier for ZrO_2 on silicon even in the presence of large depolarization fields arising from the presence of both the vacuum and silicon layers. This barrier contrasts with the predicted behavior of $SrTiO_3$ on silicon, where the expected small polarization barrier of strained $SrTiO_3$ disappears due to both depolarization and charge transfer at the $SrTiO_3$−Si interface.[43] The coupling of the bistable polarization to the Si carriers is revealed in calculations of the Si density of states (Figure 1d). These calculations show that the density of states is energetically shifted by ∼0.6 eV with respect to vacuum when the polarization is switched.

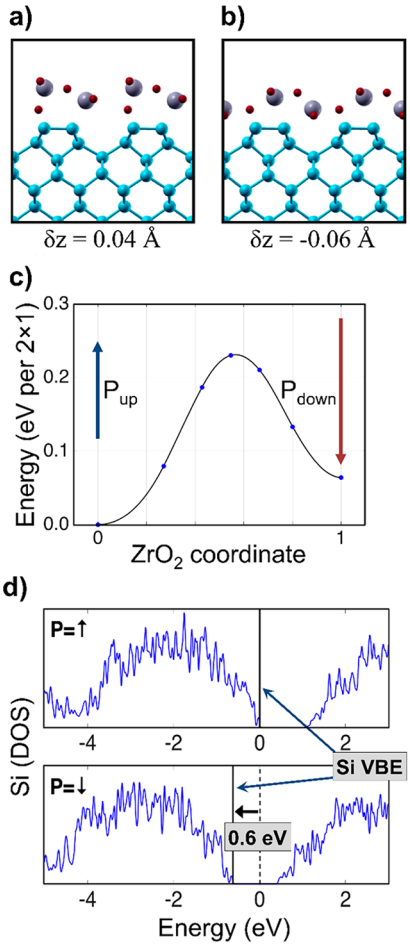

Figure 1. Two of the lowest energy structures for the ZrO_2 monolayer on Si (001) surface. Si atoms are shown in cyan, Zr atoms in gray, and O atoms in red. The physical structures computed using DFT for two configurations of the ZrO_2 monolayer have opposite out-of-plane polarizations. The polarization for each calculation is parametrized by δz: the average {001} coordinate of the Zr atoms minus the average {001} coordinate of the O atoms. (a) Upwardly polarized structure has δz = +0.04 Å while the (b) downwardly polarized structure has δz = −0.06 Å. (c) Energies of the structures that lie on the minimum energy transition path between these two structures are calculated via the nudged elastic bands (NEB) method.[40] The energy barrier is computed using five intermediate states, shown as blue dots. The curve that interpolates between these states is a polynomial fit. The "down" polarization state is 0.07 eV (per 2 × 1 surface unit cell) higher in energy than the "up" polarization state, and the energy barrier is 0.23 eV (per 2 × 1 surface unit cell). The blue arrows represent the polarization vectors as measured by δz for the two states. The 2 × 1 unit cell contains two ZrO_2 formula units. (d) Density of states in an interior Si layer shows a valence band edge (VBE) shift between the "up" state (top) and the "down" state (bottom).

To guide the experimental realization of ferroelectric ZrO_2, we examine the structural features of the ZrO_2 monolayer that give rise to switchable polarization. Because of the rich landscape of stable configurations at low energy with similar chemical bonding and small structural differences, the theory predicts that growing single crystalline epitaxial films of ZrO_2 on Si(001) should be challenging. However, epitaxy may not be a necessary condition for ferroelectricty in this system. A close examination of the structures shown in Figure 1 indicates that the symmetry of the silicon surface, as well as the inherently rumpled structure of ZrO_2, gives rise to the switchable

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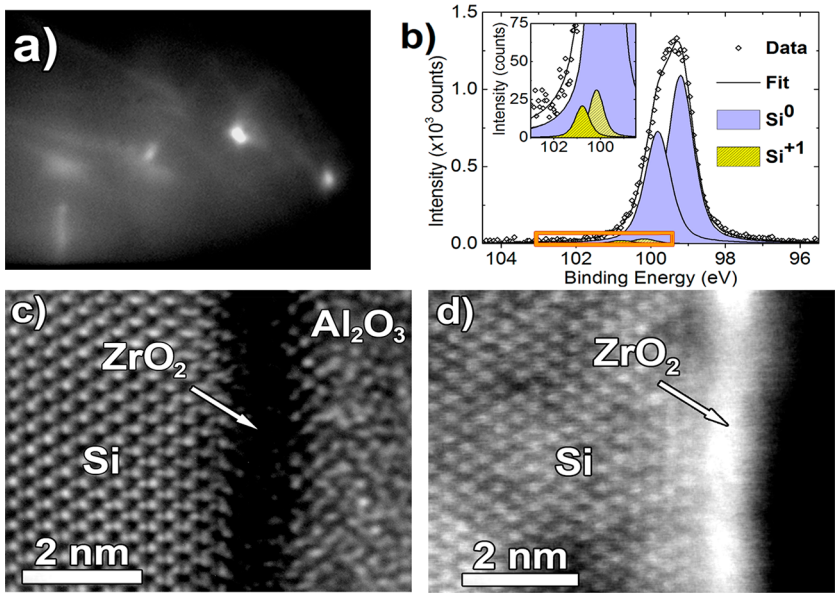

Figure 2. Physical properties of the Si-oxide interface. (a) RHEED image of the ZrO_2 monolayer prior to Al_2O_3 deposition. (b) Si 2p XPS spectrum of a ZrO_2/Si interface covered with a thin (3 nm) a-Al_2O_3 layer. The inset shows a magnification of the Si^{1+} region taken from the orange rectangle. (c) TEM and (d) HAADF STEM micrographs of the cross section of an a-Al_2O_3/ZrO_2/Si stack.

polarization. The switching of the dipole occurs by a continuous displacement of a group of atoms in the unit cell, while one oxygen remains in place. No significant chemical change occurs during this transition. From the structure, we note that open channels in the (001) face of silicon allow for the motion of the oxide atoms lacking silicon nearest neighbors, which stabilizes the two polar ZrO_2 structures.

One key implication of this finding is that an epitaxial system is not required for ferroelectricity; only an atomically abrupt structure with silicon is needed. This essential finding significantly relaxes materials processing requirements, allowing us to explore alternate routes to synthesize monolayer ferroelectrics on silicon, including partially *amorphous* systems as well as using a variety of deposition methods, such as atomic layer deposition.[14] We test this idea experimentally by depositing a ferroelectric gate stack of monolayer ZrO_2 on Si that is atomically abrupt but not necessarily epitaxial. The ZrO_2 is grown using a reactive evaporation system, on top of which we deposit a-Al_2O_3, which replaces the vacuum in the calculation and supports an applied electric field for switching the ZrO_2. The choice of a-Al_2O_3 as a gate oxide is based on its excellent insulating properties including low-leakage and ease of growth.

To grow ZrO_2 on silicon with an atomically abrupt interface, we first wet clean the silicon substrate, remove the native surface oxide using 5% HF/H_2O, and expose the resulting hydrogen-terminated Si surface to UV-ozone to regrow SiO_2 back on the surface to a thickness of approximately 0.5 nm. We then deposit one monolayer of Zr metal on top of the SiO_2 using an electron-beam (e-beam) source in a background pressure of $\sim 5 \times 10^{-9}$ Torr. To remove the SiO_2, we heat in vacuum until the SiO_2 desorbs, typically for <2 min at 870 °C. Desorption of the SiO_2 is monitored using reflection high-energy electron diffraction (RHEED) and is complete when the background signal decreases (Figure 2a). The gate stack is completed with a layer of a-Al_2O_3 deposited by thermally evaporating Al at $\sim 8 \times 10^{-7}$ Torr O_2, with the substrate kept at room temperature.

To verify that this process results in an atomically abrupt interface of ZrO_2 on silicon (without SiO_2 at the interface), we use X-ray photoelectron spectroscopy (XPS). A sample with a thin (3 nm) a-Al_2O_3 layer on top of ZrO_2 is moved in vacuo between the deposition and XPS analysis chambers. The effectiveness of the procedure to form an abrupt ZrO_2−Si interface is demonstrated by the dominance of the nonoxidized Si^0 component in the Si 2p spectrum, as shown in Figure 2b. The relative area of the Si^{1+} component is ~2.5% with respect to the Si^0 peak. From the XPS data, the amount of the suboxide is found to be less than 0.2 monolayers of Si^{1+}.[44] A feature observed at a lower binding energy (~98.4 eV) may be the result of a small number Zr−Si bonds at the ZrO_2−Si interface.[45] A cross-section transmission electron microscope (TEM) micrograph (Figure 2c) and a scanning TEM (STEM) high-angle annular dark field (HAADF) micrograph (Figure 2d) of a (22 nm)a-Al_2O_3/(1 nm)ZrO_2/Si sample show that the ZrO_2 layer is uniform and continuous, with a sharp interface with Si. This observation is further supported by elemental line profiles (Figure S1, Supporting Information).

Capacitor devices are fabricated from the as-grown gate stack of (50 nm)Pt/(22 nm)a-Al_2O_3/(1 nm)ZrO_2/Si. The capacitance−voltage (C−V) behavior shown in Figure 3 demonstrates ferroelectric switching of the ZrO_2 interface. As a control, we also deposit a gate stack with 12 nm-thick a- Al_2O_3 using the same procedure described above, from wet cleaning to vacuum anneal, but without ZrO_2 at the interface. The control sample (Figure 3, inset) shows C−V behavior typical of a metal oxide semiconductor (MOS) capacitor. At negative voltages, the Fermi level of the silicon at the oxide−silicon interface is near the Si valence band, and holes accumulate at the interface so that the measured ac capacitance is only that of the oxide gate stack. As the voltage is increased, the Fermi level at the interface moves into the silicon band gap, depleting charge at the interface; the capacitance decreases due to the added capacitance from the silicon depletion layer.

The striking feature of the C−V characteristics for the gate stack with ZrO_2 at the interface (Figure 3) is hysteretic

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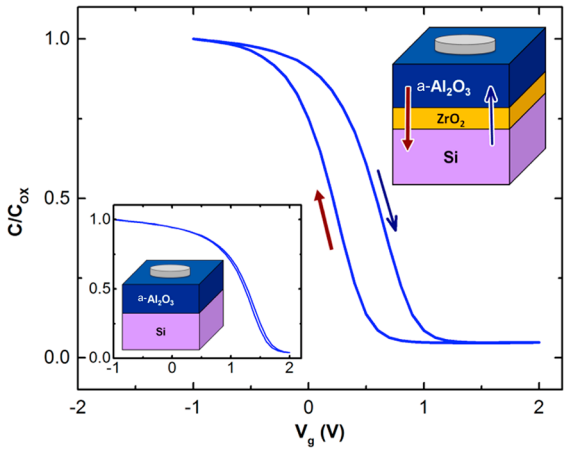

Figure 3. Ferroelectric behavior of ZrO_2 on Si. A capacitance−voltage (C−V) curve of a Pt/a-Al_2O_3(22 nm)/ZrO_2(1 nm)/Si MOS capacitor with the capacitance normalized to the capacitance in accumulation (C_{ox}), with arrows indicating the scan direction. The top inset shows a schematic device structure with the polarization corresponding to the arrows marking the sweep direction. The bottom inset shows a C−V curve of a control sample with 12 nm a-Al_2O_3 and no ZrO_2 layer.

behavior. This behavior is notably absent in the control sample that does not include the ZrO_2 layer (Figure 3 inset). The sense of the hysteresis, indicated by the arrows in Figure 3, is consistent with ferroelectric switching of the ZrO_2 and a concomitant change in the Si Fermi level,[6] as predicted by DFT (Figure 1). The magnitude of the hysteresis, ∼0.4 V, is slightly smaller than the ∼0.6 eV predicted by DFT (Figure 1d), which is explained if only a fraction of the ZrO_2 in the amorphous structure switches. The hysteresis in the C−V behavior shows a switchable dipole at the interface: the field and polarization of the ZrO_2 point downward at negative voltages. As the field across the ZrO_2 increases in the positive direction during the voltage sweep, the polarization of the ZrO_2 flips from down to up. This change in polarization induces a positive switchable field at the interface and shifts the C−V curve toward negative voltages, as observed in Figure 3.

While ferroelectric switching is observed, the down state of the ZrO_2 ferroelectric eventually reverts to the up state, as observed by a shift of the C−V curve with time. This decay is analyzed by applying a 2 V bias to the gate to prepare the ZrO_2 in the down state, immediately followed by measurement of the capacitance as a function of time at a bias of 0.2 V, which is where the C−V curve shows the largest capacitance difference for the two polarization states. At this voltage, the capacitance is observed to increase to 50% of the up state capacitance after 10 min. The relaxation from the down state to the up state is a consequence of the predicted metastability of the down state (see Figure 1c). The relaxation time depends on the kinetic barriers and detailed mechanisms for polarization relaxation. Future work on processing routes to improve the retention time will focus on manipulating the relaxation energy barrier by modifying the growth process of the ZrO_2 layer and changing the amorphous capping layer. Finally, we note that by tuning the thickness of the a-Al_2O_3 layer and other capacitances in the stack, a negative capacitance regime may be possible that would reduce the required voltage to operate the MOSFET and thus dramatically lower the amount of dissipated energy.[34,35]

In summary, we demonstrate that a monolayer ferroelectric can be fabricated at an atomically abrupt ZrO_2−Si interface. For a stack that incorporates ZrO_2, first-principles theory predicts the magnitude of the switching to be 0.6 V, a value verified by C−V measurements. The essential structural element that gives rise to the switchable dipole is a rumpled ZrO_2 structure and an open structure in the silicon surface. This feature allows ZrO_2 to serve as a switchable dipole when incorporated into an amorphous gate stack that is more conducive to manufacturing than an all-epitaxial stack.

Theoretical Section. We employ density functional theory (DFT) in the generalized gradient approximation (PBE GGA)[46] with ultrasoft pseudopotentials,[47] using the QUANTUM ESPRESSO software package.[48] We use a plane wave energy cutoff of 35 Ry and an 8 × 8 Monkhorst−Pack Brillouin zone mesh (per 1 × 1 surface cell) with a Marzari-Vanderbilt smearing of 0.02 Ry for electronic temperature.[49] A simulation supercell comprises 16 atomic layers of Si with a bottom layer passivated with H, a monolayer of ZrO_2 neighboring the top surface of Si, and ∼12 Å of vacuum to separate periodic copies of the system in the {001} direction. The lattice constant in the (001) plane is fixed to the DFT-computed bulk Si lattice constant of 3.87 Å. All atoms are relaxed (except the bottom 4 layers of Si, which are fixed to represent the bulk) until the forces on the atoms are less than 10^{-3} Ry/a_0 in all axial directions. Since the simulation cell is asymmetric in nature, the system has a total dipole moment due to the polarization of the oxide, which can interact with the dipole moments of its periodic copies. To prevent this spurious electrostatic effect, we employ a fictitious dipole in the vacuum region of the cell, which is self-consistently calculated so that it flattens the electrostatic potential in vacuum.[50]

Experimental Section. P-type Si wafers (B-doped, ∼6 × 10^{15} cm^{-3}) are cleaned by immersing the wafer in H_2O_2/H_2SO_4 (1:3) at 130 °C followed by a deionized water (DI) rinse. The native oxide layer is removed in a dilute (3:70) HF solution in DI for 1 min. The wafer is then placed under a UV−ozone lamp for 30 s and immediately transferred to a UHV system. The UV−ozone treatment results in a thin, 0.5 nm-thick layer of SiO_2 on the surface, as determined using XPS.

Prior to Zr metal deposition, the substrates are annealed at <10^{-9} Torr at 400 °C for 20 min to desorb moisture and hydrocarbons. One monolayer of Zr is evaporated with an e-beam source at ∼5 × 10^{-9} Torr, with the substrate kept at room temperature. Deposition rates are calibrated using a quartz crystal monitor. The sample is annealed for 2 min at 870 °C at <10^{-9} Torr. From the XPS results, this step desorbs any remaining SiO_2, and the oxygen reacts with Zr to form ZrO_2. After cooling, an O_2 leak valve is opened, and Al_2O_3 is grown by evaporating Al from a thermal source in ∼8 × 10^{-7} Torr O_2, with the substrate kept at room temperature. The control sample is prepared in the same way. MOS capacitors are prepared by e-beam deposition of 50 nm Pt through a shadow mask without exposure to air.[51] C−V measurements are done ex situ on pads with an area of 5.15 × 10^{-5} cm^2 at a frequency of 1 MHz and using 100 mV voltage steps. A positive V_g is a positive voltage applied on the Pt gate with respect to the back of the wafer, which is contacted with an indium−gallium alloy.

X-ray photoelectron spectroscopy is performed in situ using an Al Kα source (1486.6 eV) on samples with a 3 nm layer of a-Al_2O_3. Peak fitting is done using XPSPEAK 4.1 with a Shirley-type background, a 50% Gaussian−Lorentzian ratio, and a 0.61 eV doublet separation for Si 2p peaks. The energy scale is calibrated to the Au $4f_{7/2}$ core level peak. TEM sample preparation is carried out using conventional polishing of a

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wedge sample. TEM and HAADF STEM imaging are performed using an FEI Tecnai Osiris operated at 200 keV, equipped with a Bruker Quantax EDX detector.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.nanolett.7b03988.

Data and analysis of interfacial elemental distribution at $Al_2O_3/ZrO_2/Si$ interface (PDF)

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Notes

The authors declare no competing financial interest.

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