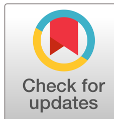

Epitaxial Oxides on Semiconductors: from Fundamentals to New Devices

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Abstract

Functional oxides are an untapped resource for futuristic devices and functionalities. These can range from high temperature superconductivity to multiferroicity and novel catalytic schemes. The only route for transforming these ideas from a single device in the lab to practical technologies is by integration with semiconductors. Moreover, coupling oxides with semiconductors can herald new and unexpected functionalities that exist in neither of the materials. Therefore, oxide epitaxy on semiconductors provides a materials platform for novel device technologies. As oxides and semiconductors exhibit properties that are complementary to one another, epitaxial heterostructures comprised of the two are uniquely poised to deliver rich functionalities. This review discusses recent advancements in the growth of epitaxial oxides on semiconductors, and the electronic and physical structure of their interfaces. Leaning on these fundamentals and practicalities, the material behavior and functionality of semiconductor-oxide heterostructures is discussed, their potential as device building blocks is highlighted. The culmination of this discussion is a review of recent advances in the development of prototype devices based on semiconductor-oxide heterostructures, in areas ranging from silicon photonics to photocatalysis. This overview is intended to stimulate ideas for new concepts of functional devices and lay the groundwork for their realization.

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1. Introduction

1.1. Background and Motivation

The heterojunction formed between a semiconductor and an oxide is one of the most technologically important inventions ever developed. Starting with SiO_2 and now HfO_2, the oxide layer acts as an insulating dielectric that enables the surface potential of the semiconductor to be modulated through applied electric fields. This basic functionality in what are known as metal-oxide-semiconductor (MOS) devices underpins the operation of field-effect transistors (MOSFET) that have revolutionized information processing. Despite this success or perhaps because of it, the functionality of the semiconductor-oxide heterojunction has remained largely within the MOS paradigm since its inception.

In this regard, advances in epitaxial growth have opened pathways to introduce new functionalities to semiconductor-oxide heterojunctions. Single crystalline oxides can now be grown on semiconductors ranging from Si to GaN. Particularly noteworthy is the integration of perovskite structured (ABO_3) oxides on (001) surfaces of diamond cubic or zincblende structured semiconductors, such as Si and GaAs. Referred to as multifunctional oxides, a wide variety of material behaviors can be realized by altering the composition of the A- and B-site cations within the basic ABO_3 structure of these materials. Such properties include piezoelectricity, ferroelectricity, ferromagnetism, metal insulator transitions and related behaviors that stem from strong electron-electron and electron-lattice correlations. Yet more intriguing, the common perovskite structure enables compositionally dissimilar oxides to be monolithically combined in layered heterostructures. If the properties of oxides and layered heterostructures can be properly harnessed, the semiconductor-oxide heterojunction could transcend the MOS paradigm and impact applications ranging from energy harvesting to nanophotonics.

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At the most basic level, the epitaxial growth of crystalline oxides on semiconductors provides a pathway for these materials to be integrated on technologically relevant platforms. Oxides per se exhibit properties that are not found in conventional semiconductors, such as multiferroicity, spin-polarization, colossal magnetoresistance and metal-insulator transitions. Silicon remains foremost the ideal physical platform by which oxides can be introduced to device technologies, as cost-effective approaches to produce large scale single crystal oxide substrates are presently not available. In principle, integration on Si enables the functionality of oxides to be exploited in complementary MOS technology and microelectromechanical systems (MEMS).

Progressing to the next level are functionalities that emerge by coupling the electrical properties of oxides with those of semiconductors. MOS functionality is the most basic yet essential form of electrical coupling between an oxide and semiconductor. Given the broad range of electronic properties of multifunctional oxides, MOS functionality is just one of several functionalities that could potentially emerge in semiconductor-oxide heterojunctions. The motivation for electrically coupling oxides to semiconductors can be understood by examining their respective electronic properties. Oxides exhibit material properties that are not found in conventional semiconductors, such as the aforementioned behaviors of multifunctional oxides. In comparison, semiconductors exhibit material characteristics that are difficult to find in oxides, such as high carrier mobilities at room temperature, long spin coherence times, direct band-gaps, and the ability to exhibit bipolar conduction. The complementary relationship in material properties between semiconductors and oxides fundamentally stem from their respective covalent and ionic natures. Thus, epitaxial heterojunctions comprised of multifunctional oxides and semiconductors could, in principle, exhibit the "best-of-both-worlds", namely, properties or functionalities that cannot be realized using either material alone. This synergistic approach to materials engineering could help address emerging technological challenges in which both ionic and covalent material characteristics are needed.

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Examples include emergent ferroelectricity (with non-ferroelectric oxides), various tunnel junctions, and most recently, the ability to leverage oxide-semiconductor interface for photoelectrocatalytic water splitting.

1.2. Scope and Overview

This review is organized into three main topic sections covering (i) the growth, physical and electronic structure in Section 2; (ii) behavior and functionality in Section 3; and (iii) emerging device applications of epitaxial oxides on semiconductors in Section 4. The sections are written in a manner so as to be largely self-contained, such that the reader can choose to read a particular topic area without needing to consult the entire review.

For the first part of the review discussing the growth, physical and electronic structure of epitaxial oxides on semiconductors, we will focus our discussion on epitaxial growth on Ge, GaAs and GaN. We refer the reader to recent reviews covering the growth of perovskite oxides on Si via molecular beam epitaxy[1–4] (MBE). We will also discuss recent advancements that have enabled epitaxial oxides to be grown on semiconductors using atomic layer deposition (ALD) and so-called hybrid MBE techniques with potential for scalability. This section will also discuss the physical structure of epitaxial oxides on semiconductors, particularly in the ultra-thin limit in which structural distortions in the oxide can be induced. We will also review the electronic structure, namely, band alignment between semiconductors and oxides.

In the second part of the review, we will discuss the behavior and functionality of epitaxial oxides on semiconductors, which provide potential “building-blocks" for the creation of device technologies. We will discuss functionalities that emerge from electrical coupling between the oxide and semiconductor, as well as functionalities that involve the oxide only. Examples of the former include

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MOS, ferroelectric-semiconductor heterojunctions, and recent advancements in engineering band-alignments, charge transfer and built-in electric fields across heterojunctions. Examples of the latter include the integration of single compound correlated oxides on semiconductors (e.g. metallic $SrRuO_3$, colossal magnetoresistive/half metallic doped manganites, superconducting cuprates) as well as more complex multi-layered heterostructures that exhibit high density electron gases (e.g. $LaAlO_3/SrTiO_3$ on Si).

In the third part of the review, we will discuss emerging device applications based on epitaxial oxides on semiconductors. Here we will begin to see the broad impact that epitaxial oxides on semiconductors could potentially have on technological development. Examples include microelectromechanical systems (MEMS) for actuation and sensing, ferroelectric-based optical modulators for silicon photonics, and heterojunctions for photocatalysis.

We conclude the review by discussing remaining challenges pertaining to the three topic sections. It should be noted that about a half of the references of this review were published in the last five years, which illustrates both our intention to focus on the most recent progress, and further provides evidence of the momentum this field has gained in recent years. We hope this review will provide further impetus in addressing remaining challenges so that the full technological potential of epitaxial oxides on semiconductors can be realized.

We focus this review on epitaxial oxides; the physical properties of amorphous and polycrystalline complex oxides are in most cases, inferior to their epitaxial crystalline analogues. For example, grain boundaries in polycrystalline oxides constitute defects that scatter electrons and smear or degrade many correlated electron phenomena and other functional properties. Moreover, the sensitivity of interface-coupled functional properties to the composition and crystal orientation at oxide-oxide and oxide-semiconductor interfaces requires atomically-abrupt crystalline interfaces. Our discussion therefore focuses on well-defined epitaxial interfaces that preserve the maximum degree of

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functional behavior. Future trends into technological commercialization may very well use oriented polycrystalline structures or amorphous layers, and some trends, such as chemical solution methods (Section 2.1.7) will be mentioned briefly.

1.3 Some Semiconductor Properties

Some of the key properties of the common semiconductors are presented in **Table 1,** alongside their relations to oxide epitaxy. The properties of $SrTiO_3$ (STO) are listed as well, being the most common oxide semiconductor in this field, and one of the most important components of oxide epitaxy on semiconductors. Since diamond is considered an interesting wide-bandgap semiconductor, this work reviews oxide epitaxy on it and it is included in the table as well.

Table 1. Selected semiconductor parameters.[5,6]

Parameter (at 300 K)	Si	Ge	GaAs	GaN	Diamond	$SrTiO_3$ (crystals)
Bandgap (eV)	1.12, indirect	0.67, indirect	1.42, direct	3.44, direct	5.47	3.2, indirect
Structure	Cubic, diamond	Cubic, diamond	Cubic, zinc blende	Hexagonal, wurzite	Cubic, diamond	Cubic, perovskite
Lattice constant (A)	5.431	5.646	5.653	a=3.189 c=5.182	3.569	3.905
Bulk electron mobility ($cm^2V^{-1}s^{-1}$)	1,450	3,900	8,000		1,800	~5
Bulk hole mobility ($cm^2V^{-1}s^{-1}$)	500	1,900	400		1,200	
Dielectric	11.9	16.0	12.9	10.4	5.7	~300 (low

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constant						field) [7]
Thermal conductivity ($Wm^{-1}K^{-1}$)	156	60	45	2~3	1000	~12 [8]
Epitaxial relation		$(001)_F\|\|(001)_S$ $[110]_F\|\|[010]_S$		$(111)_F\|\|(0001)_S$ $[1\text{-}10]_F\|\|[11\text{-}20]_S$	$(001)_F\|\|(001)_S$ $[010]_F\|\|[110]_S$	
Most common oxide (lattice mismatch#)	STO (+1.6%)	BTO (<0.1%), a-axis (1.1%), c-axis STO (-2.2%)	STO (-2.3%)	STO on TiO_2	EuO (+1.8%)	
Conduction band offset& (eV)	0 – (-0.8) [9,10]	BTO: 0.0 [11] STO: (-0.1)-(-0.4) [12]	(-0.7) [13]	TiO_2: 0.05 [14]		
Valence band offset& (eV)	-2.2 – (-3.0) [9,10]	BTO: (-2.6) [11] STO: (-2.7)-(-3.0) [12]	2.5 [13]	TiO_2: (-0.4) [14]		

Positive values refer to compressive strain.

& Positive values refer to the relevant band being higher in the oxide with respect to the semiconductor, for both types of bands.

2. Growth, Physical and Electronic Structure

2.1. Growth

Since McKee et. al. first demonstrated the epitaxial growth of the perovskite $SrTiO_3$ (STO) on the (001) surface of Si in 1998 by molecular beam epitaxy[1] (MBE, **Figure 1a**), an intense research effort has been devoted to extending the combination of epitaxial complex oxide materials which can be synthesized in single crystal form on semiconductor substrates. A critical step in integrating

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multifunctional complex oxides with semiconductors involves the development of synthesis techniques which overcome major challenges related to growth. These challenges include circumventing the oxidation of the semiconductor surface and reducing the thermal budget for the metal oxide growth, while ensuring the growth of stoichiometric crystalline oxide phases with minimal defects. Thus, the growth window for the epitaxial growth of oxides on semiconductors must take into account the thermal, lattice and symmetry mismatch between the film and the substrate.[1,3,15,16] Key to this progress has been the understanding of the chemical interactions between alkaline earth metals and semiconductor surfaces such as Si which has led to the discovery of effective template layers for oxide epitaxy.

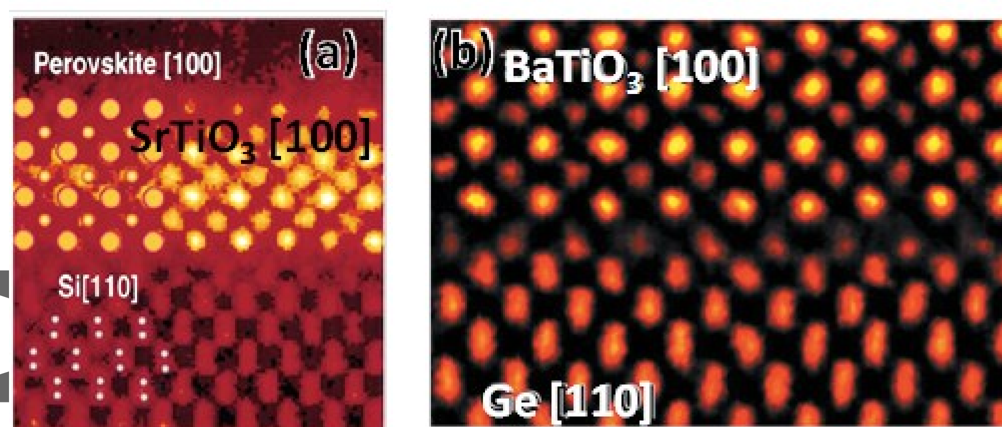

Figure 1. The first reports of an epitaxial (a) $SrTiO_3$ on Si[1] and (b) $BaTiO_3$ on Ge,[17] both grown using MBE. Reproduced with permission.[1] Copyright 1998, American Physics Society. Reproduced with permission.[17] Copyright 2001, The American Association for the Advancement of Science, respecitvely.

MBE remains the most common technique for oxide epitaxy on semiconductors. It provides precise control over kinetic and thermodynamic conditions needed to achieve high crystalline and interfacial quality. Complementary techniques, such as atomic layer deposition (ALD), offer considerable

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potential for higher throughput and scalability. We will begin this section with MBE growth, and then describe more recent approaches such as hybrid MBE-ALD, hybrid (organic-inorganic) MBE, and pulsed laser deposition (PLD).

At the oxide-semiconductor interface, chemical interactions between the semiconductor and the oxide lead to transfer of electrons from semiconductor to the more electronegative oxygen in the interfacial oxide layer. A consequence of this charge transfer is the formation of an intrinsic dipole at the oxide-Si interface. The effect of this dipole on the atomic-scale structure and the electronic band offsets at the oxide-semiconductor interface has been investigated theoretically and experimentally, and the major findings are summarized below.

Finally, the realization of atomically abrupt oxide-semiconductor interfaces has important implications for coupling the symmetries of reconstructed semiconductor surfaces with structural modes in the oxide epilayer. This interfacial interaction has exciting prospects for modulating the physical properties of oxide thin films where a strong coupling of structural degrees of freedom with technologically important electronic and magnetic phases exists. We discuss the $BaTiO_3$/(2×1)Ge (BTO/Ge) interface where non-bulk phases are stabilized. First principles calculations predict non-volatile switching of polarization state of the BTO and the band offset between the BTO and Ge.

2.1.1. Molecular Beam Epitaxy of Oxides on Si and Ge

McKee and co-workers first demonstrated that the growth of an alkaline earth template layer on the clean reconstructed semiconductor surface serves as an effect buffer for the commensurate growth of complex oxide films using the molecular beam epitaxy (MBE) technique[1] (Figure 1a). The key to the success of this approach lies in the relative thermodynamic stability of the alkaline earth silicide that prevents oxidation of the underlying Si substrate. Here, a ½ monolayer of the alkaline earth metal is

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initially deposited at ~650 °C forming an ordered commensurate stable silicide structure as evidenced by reflection high energy electron diffraction.

The growth of the initial oxide layers requires low temperatures and oxygen pressures (relative to typical growths of oxides) to avoid oxidation of the Si substrate. A variety of steps have been developed for the growth of $SrTiO_3$ (STO) on Si to achieve this stringent requirement.[3] Following the deposition of the ½ Sr template layer, an additional monolayer of SrO is grown by depositing Sr in a low oxygen pressures and low temperature. This step is followed by the growth of an amorphous STO layer at low temperatures, which is then recrystallized by a UHV anneal.[18–20] This provides a template layer that allows for the consequent growth of transition metal oxides over a wide range of oxygen pressures and growth temperatures without the formation of an amorphous SiO_2 interfacial layer. Similar steps have been used to grow $BaTiO_3$ (BTO) on Ge using ½ ML Ba or Sr as the Ge passivation layer[17,21] (Figure 1b). After the initial ½ ML Sr Zintl template is grown on Ge, Fredrickson et al. show that the initial BTO layers can be grown at 650 °C by progressively increasing the oxygen pressure.[22]

In general, the common thread of growth of oxides on semiconductors is based on separating the steps requiring oxygen from the steps requiring high temperature, as means for mitigating surface oxidation of the semiconductor surface. This is achieved by the low-temperature deposition of STO on the Zintl-stabilized semiconductor surface, and then annealing it in UHV. The careful control and limit of the oxygen pressure during growth is not only about keeping it low; too low oxygen will not only form a defective oxide, but may cause a silicide reaction between the semiconductor and metallic atoms, if the latter are not sufficiently oxidized. This subsection provides a short glimpse of the many aspects of MBE growth, and we refer the readers to a recent book that thoroughly addresses the manner.[3]

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Following the breakthrough work of McKee at al, additional strategies have been developed to integrate oxides with semiconductors using MBE, pulsed laser deposition (PLD) and atomic layer deposition (ALD), as will be discussed over the next sections.

2.1.2. Atomic Layer Deposition

Atomic layer deposition (ALD) is a widespread, self-limiting thin film deposition method with high flexibility, and excellent coverage of complex 3D structures with high aspect ratio.[23] ALD is a highly scalable technique, with dozens of large wafers accommodated in commercial systems. While this method is popular for deposition of amorphous oxides such as Al_2O_3 and HfO_2, ALD is suitable for a wide range of materials ranging from metals to sulfides, nitrides and many other compounds, including perovskite oxides.[24] A key application of ALD is deposition of Hf oxide high-k dielectrics in advanced microelectronics technologies.[25,26] Since its first days ALD has been used for epitaxy, and later on it has been applied for oxide epitaxy. More recently, after considerable development by the community, ALD has been successfully applied for oxide epitaxy on semiconductors. This approach promises a scalable, low-cost alternative to MBE, which may herald the maturation of practical device applications from the physics that we review in this paper. Carbon contamination from the ALD precursors remains a significant concern, however, recent reports indicate that post-growth anneals are effective in reducing carbon-related defects. We present here a few key examples, and refer the interested reader to a 2015 review by McDaniel et al. that thoroughly covers this exciting field.[27]

All ALD $SrTiO_3$/Si

Ideally, an all-ALD process will be preferable for the scalable integration of functional oxides with semiconductors. Hence, the development of ALD-compatible buffer layers which maintain structural integrity of the semiconductor interface is crucial. Zhang et. al have demonstrated the passivation of

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the Si(001) surface by ½ a monolayer of Sr using HyperSr [bis(triisopropylcyclopentadienyl)Sr, or: $Sr(C_5Pr_3H_2)_2$] and H_2O as precursors, followed by a high temperature (800-850 °C) anneal.[28] The consequent growth of high quality films on the ALD-grown Sr-Si templates remains challenging to date due to difficulties in mitigating the formation of an interfacial SiO_2 layer.[27] To circumvent this limitation, it has been shown that ALD growth of STO can be achieved on STO buffer layers grown by MBE, which is termed *hybrid MBE-ALD growth*.

Hybrid MBE-ALD Growth of $SrTiO_3$*/Si*

McDaniel and coworkers have demonstrated the homoepitaxial growth of STO films by ALD using HyperSr, titanium tetraisopropoxide (TTIP), and water as the precursors at moderate 250 °C growth temperature on 4 unit-cells of MBE-grown STO templates on Si(001). Carbon contamination from the ALD cycles were effectively removed by a vacuum anneal at 250 °C as evidenced by XPS measurements without the reduction of the STO.[29] This work constitutes a promising start, but owing to the considerable tendency of Si for oxidation, it remains unclear whether all-ALD processes could yield oxide epitaxy on Si in the future.

ALD Oxides on Ge

An alternative substrate for ALD oxide epitaxy is Ge. Oxides of Ge have a lower oxide stability than oxides of Si, hence, a larger growth window is expected for the realization of metal oxide-semiconductor interfaces with minimal GeO_x. McDaniel and coworkers have demonstrated direct ALD growth of crystalline STO and $SrHfO_3$ (SHO) films, with atomically abrupt interfaces on Ge. Following the removal of the native oxide from the Ge substrate, the ALD deposition of amorphous STO and SHO films at 225 ^{o}C and a subsequent anneal in vacuum or 10^{-6} Torr P_{O2} at 585-650 ^{o}C for 5

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minutes results in crystalline oxide films[30] (**Figure 2a**) Thicker oxides films (~15nm) were synthesized using the two-step low temperature deposition and high temperature anneal procedure. X-ray photoelectron spectroscopy (XPS) and transmission electron microscopy measurements confirm the absence of an interfacial GeO_x layer (Figure 2b).

MOS structures based on the ALD grown STO/Ge possess a high dielectric constant of ~90 but exhibit high-leakage currents (10A/cm^2 at 0.7 MV/cm) due to the small conduction band offset of ~0.12 eV between STO and Ge. The leakage current can be inhibited by Al-doping. Al-doped STO films grown on undoped STO buffer layers by ALD exhibit a two orders of magnitude reduction in the leakage current due to the increase in the oxide band gap by Al doping. Section 3.1.2. further discusses the electrical properties of these structures as high-k dielectrics.

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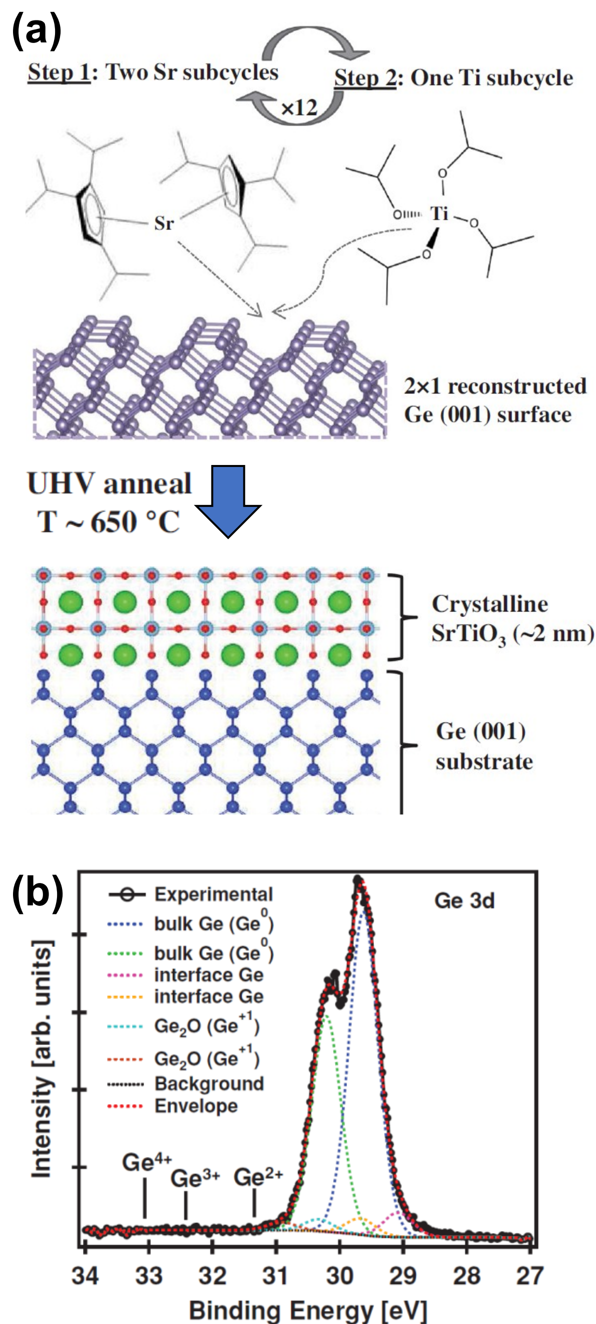

Figure 2. ALD STO/Ge. a) Schematic of the deposition process showing the precursors reaching the dimerized Ge surface, and the formation of an epitaxial oxide following anneal. b) An XPS analysis showing the absence of oxidized Ge near the interface. Reproduced with permission.[30] Copyright 2014, Wiley-VCH.

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ALD $SrHfO_3$/Ge

McDaniel and coworkers further demonstrated that crystalline $SrHfO_3$ films can be grown on clean 2×1 Ge(001) surfaces with low leakage currents[31] (6×10^{-6} A/cm^2 at an applied field of 1 MV/cm, equivalent SiO_2 thickness of 1.0nm, k=20). SHO has a large bandgap of 6.1 eV with a 2.2 eV conduction band offset with Ge and a valence band offset of 3.2 eV. More on the electrical characteristics of this system can be found in Section 3.1.2.

Hf doping of STO, forming $SrHf_xTi_{1-x}O_3$ (SHTO) films on Ge has been used as a route to increase the band offsets and engineer the strain states from 2.2% for STO to -1.9% for SHO. Atomically sharp interfaces have been obtained with ALD.[32] The crystallization temperature is found to increase from 520 °C for STO to 640 °C for SHO. Both 2×1 and 1×1 interfaces are observed in high resolution scanning transmission electron microscopy (STEM) images for an SHTO (x=0.55) where the 2×1 structures are characterized by the presence of ½ ML Sr compared with 1 ML Sr for the 1×1 interfaces. While the leakage current increases for x=0.55 to 0.1 A/cm^2 compared to ~10^{-5} A/cm^2, for SHO the dielectric constant increased to 30.

ALD $SrZrO_3$/Ge

To reduce the leakage current, $SrZiO_3$ (SZO) films were epitaxially grown on Ge with ALD by Hu and coworkers[33] with an equivalent SiO_2 thickness of 0.8 nm and k=30. The ALD SZO films were grown either directly on Ge or on MBE-grown Ba Zintl templates which were transferred in-situ from the MBE chamber to the ALD reactor. It was previously found that the Ba-Zintl template forms an effective barrier to prevent carbon contamination of the Ge surface.[34] Following the deposition of a 3 nm SZO buffer annealed at 590 °C for crystallization, additional crystalline SZO layers could be deposited at 225 °C.

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2.1.3. Pulsed Layer Deposition of $SrTiO_3$/Si

Pulsed laser deposition (PLD) is currently the most common tool for oxide epitaxy on oxide substrates, owing to its relative ease of operation and wide span of possible materials.[35,36] While it is not as scalable or industry-compatible as ALD, and the energertics and typical high growth pressures are challenging for oxide/semiconductor epitaxy, the widespread use of PLD in research, and efforts to increase its scalability,[37,38] make it potentially attractive for oxide epitaxy on semiconductors.

Spreitzer et al. have looked beyond these hurdles and published their first attempt at PLD growth of STO/Si in 2013.[39] Since then, a continuous improvement in the film quality has been demonstrated. The PLD chamber has been equipped with a vacuum system enabling a base pressure of ~10^{-8} Torr, which is lower than typical oxide PLD processes. A metallic Sr target has been employed for the initial 1/2 monolayer of Sr passivation of the Si surface. Similarly to growth on Si, it was shown that the understanding and precise control of the structure and reconstructions of this initial Sr Zintl phase, and its evolution, are critical for obtaining STO epitaxy.[40–42] This critical surface passivation, together with optimized annealing schemes, have significantly promoted higher crystalline qualities,[43,44] showing considerable progress. Even the highest quality PLD films still contain an amorphous interface layer. Yet, for quite a few of the applications described in this paper – several nm of interface layer form even with MBE films that started the best initial interface quality, due to subsequent processing.

Further progress in PLD oxide epitaxy on Si is expected to drive the field forward by opening it to many research groups that can only grow on oxide substrates today. In addition, other semiconductors such as Ge are somewhat less challenging for oxide epitaxy, and we call upon the community to explore these possibilities further.

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2.1.4. Hybrid MBE $SrTiO_3$/Si

Zhang and co-workers have explored the hybrid MBE (hMBE) growth method to fabricate stoichiometric STO films on Si with scalable growth rates on the order of 1 nm/min.[45] The hMBE technique has been thoroughly detailed in a recent review.[46] Sr is evaporated from an elemental thermal source and Ti and O are obtained from an alkaloid precursor titanium tetraisopropoxide (TTIP). The growth is self-regulated, leading to an expansion of the growth window for the synthesis of stoichiometric crystalline STO films on Si. Films are grown by co-deposition of the Sr and TTIP on a ½ ML Sr-Zintl buffer layer. When employing metal-organic precursors such as TTIP, carbon contamination reaching the hot Si surface forms carbides, which even as submonolayer is detrimental to STO epitaxy. This challenge was addressed by long deposition of Sr on the chamber walls prior to growth, which serves as a getter by reacting with the residual contamination. The TTIP is then introduced only after the Sr-Zintl buffer layer has been formed, at which point the surface is much less reactive to residual carbon.

The crystalline quality of hybrid MBE STO/Si was subsequently improved by the development of a two-step anneal scheme and further optimization of the growth details.[47] Additional insights on the growth mechanism with this method has led to the development of a technique to continuously tune the epitaxial strain of STO layers grown on Si, using the thermal mismatch between the materials via the growth temperature.[48] This achievement is potentially promising as a substrate for strain engineering of other oxides, a prominent route for tuning their properties.[49]

2.1.5. Growth on GaAs

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GaAs is the second most common semiconductors after silicon, and the most common when optoelectronics are involved. GaAs is characterized by a direct band gap and high electron mobility (Table 1), and it can be readily integrated with its relatives of the III-V family, providing excellent tunability of the band structure. This is routinely performed using mature and robust technology[50] that enables synthesizing some of the highest structural and interfacial qualities of any crystalline interfaces. III-V are furthermore readily integrated with group IV semiconductors, further extending their functionality and technical maturity. As such, GaAs is an attractive candidate for integration of epitaxial oxides. However, this turned out to be a rather challenging task.

One of the unique challenges of oxide epitaxy on GaAs revolves around surface preparation. As a compound semiconductor, GaAs exhibits multiple native oxide moieties, with a wealth of structural and electronic defects and compensation mechanisms, several of which are detrimental for electronic devices. While for Si and Ge the native oxide readily desorbs by heating in UHV[3] (Section 2.1.1), this approach is not practical for III-V semiconductors. In GaAs and most III-Vs, As, or the column-V element, readily evaporates from the crystal at intermediate temperatures. In plain words, attempting to perform thermal desorption of the GaAs native oxide would result in As desorption, which may even result in Ga droplets on the surface. Alternative approaches must therefore be applied.

In GaAs technology, clean GaAs surfaces are obtained by homoepitaxial growth of GaAs films on GaAs wafers: The native oxide on the wafer is first reduced by annealing under As flux, thus preventing the loss of As from the substrate. The homoepitaxial GaAs is used to keep the electronically-active areas of devices away from residual defects at the original surface of the GaAs wafer. This same strategy is used as the preliminary step for growing epitaxial oxides.

Upon completion of the homoepitaxial GaAs layer, the most straightforward approach for oxide epitaxy is to transfer the wafer under UHV to a second growth chamber, dedicated for oxide epitaxy. To our knowledge, the Droopad group operates the single active dual-chamber system in the world that performs these growths,[51,52] due to technical complexity and cost. An alternative to a dual

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chamber system is to deposit amorphous arsenic on the surface of the homoepitaxial GaAs layer, during the last stage of the post-growth cooling. Several tens of nm of arsenic cap can protect the pristine GaAs layer from ambient oxidation, allowing the wafers to be transported in air. This tactic is well-known in the III-V community well before oxide epitaxy has been considered.[53,54] The samples can then be loaded onto an oxide epitaxy system, where the arsenic cap can be desorbed at low temperature of 300-400 °C, which is enough to desorb the amorphous As layer on the surface, but not enough to release it from the GaAs crystal. Reflectance high-energy electron diffraction (RHEED) monitoring of this step allows precise control and minimal heating, since the emergence of crystalline GaAs is immediate at the desorption temperature.[55]

Motorola has spent considerable efforts in the early 2000's growing STO/Si and STO/GaAs, in an attempt to use STO as a template for integrating these two semiconductors.[56] Liang et al., applied Ti submonolayer for passivating the GaAs surface as the first step of MBE growth of STO,[51] resulting in an atomically abrupt interface.[57] First-principle total energy calculations have subsequently explored various atomic interfacial configuration and verified that interfacial Ti stabilizes the interface, and substituting a surface Ga atom by Ti ($[Ti]_{Ga}$) stabilize the surface for both SrO/Ga and TiO/As interface terminations.[58] The opposite GaAs/STO interface has also been recently addressed by experiments and theory.[59]

Later on, it was shown that in the absence of the submonolayer Ti passivation step, a polycrystalline TiGa compound is formed at the interface, preventing the possibility of high-quality oxide epitaxy.[60] Some attempts to grow STO on GaAs using PLD have been reported,[61,62] but the crystalline quality was significantly short of that of MBE films, and they will thus not be discussed further.

Leveraging all prior expertise, high-quality STO/GaAs was demonstrated using 1/2 ML Ti for surface passivation, with detailed RHEED and XPS analysis of the structure and interface.[63] This work further explored the unconventional use of oxygen plasma instead of molecular oxygen. It

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was found that using oxygen plasma with the first few oxide layers is detrimental to the growth; however, after completing 2 nm of STO using molecular oxygen, the use of oxygen plasma for the subsequent 8 nm yielded some improvement in the crystalline quality as determined by the rocking curve. Nonetheless, the initial 2 nm of STO did not prevent the oxidation of the underlying GaAs surface: XPS and photolominescence have shown considerable degradation of the chemical and electronic properties. We therefore conclude that when the interface electronic properties are of significance, e.g., for coupled oxide-semiconductor applications, plasma is not recommended. However, this work did not address oxygen vacancies, whose presence is expected to decrease considerably when plasma is included; therefore, oxygen plasma might be worth examining for oxide-semiconductor applications where no coupling with the semiconductor is necessary 2DEGs[55] (see Section 3.5).

2.1.6 Growth on GaN

GaN and other III-Nitrides are attracting considerable attention in recent years, most notably for power electronics[64–66] and optoelectronics. This family of materials includes the $Al_xGa_{1-x}N$/GaN structures, featuring 2D electron gases[67] (2DEGs) which are particularly interesting for power and radio frequency (RF) applications.[68]

Hexagonal Wurtzite GaN is a direct wide bandgap (3.4 eV) semiconductor (Table 1). The direct bandgap makes it attractive for optoelectronics, whereas high breakdown fields, high saturation currents and large thermal conductivity make GaN attractive for high power devices.[5] Compared to Si, Ge and GaAs – GaN has considerably higher thermal and chemical stability. This stability allows some epitaxial oxides to preserve their properties on GaN at temperatures as high as 800°C,[69,70] an important aspect for device fabrication process flow and for practical integration schemes. Moreover,

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this stability is a useful feature for some elevated temperature electronics. The stability of GaN makes MBE alternatives, such as PLD and sputtering, possible for oxide epitaxy (Tables 3, 4). However, these alternatives often result in domain structure and an overall lower crystalline quality. From an oxide epitaxy point of view, despite the chemical and thermal stability advantages, ultimately the oxide crystallinities reported on GaN fall behind most of those reported for other semiconductors. This appears to be the result of crystallographic and strain limitations.

It is interesting to note that the hexagonal GaN structure can be used to epitaxially stabilize non-equilibrium oxide phases at room temperature, such as hexagonal $LaLuO_3$ [71] and monoclinic Y_2O_3 [70] (Table 3).

This section will focus on the growth of perovskites on GaN, based on STO/TiO_2 templates. Other oxides grown on GaN will be briefly mentioned in a Section 3.1.3. The growth of perovskites on GaN starts with the pioneering 2005 work of Hansen et al., who conducted a thorough investigation of epitaxial rutile-TiO_2 on GaN using MBE.[14] This work combines a description of the growth, structure and band offsets with the performance of heterojunction field effect transistor (HFET). Due to the device context, growth was conducted on AlGaN/GaN substrate, where an interfacial 2DEG serves as the channel and AlGaN acts as another insulator in series (see Section 3.1.3 for more information on the device aspects). The integration is done with the relations of $(100)_{TiO2}||(0001)_{GaN}$ and $[001]_{TiO2}||<11\text{-}20>_{GaN}$, resulting in three in-plane rotational domain variants of the oxide (**Figure 3a**). The TiO_2/GaN interface is shown to be atomically abrupt by TEM (Figure 3b), and the morphology appears to be 3D from RHEED.

These results have been leveraged by the authors as a template layer for the subsequent growth of perovskites. Tian et al. used a 30 nm rutile-TiO_2 template layer on GaN to subsequently grow 20 nm

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of (111) STO, both by MBE[72] (Figure 3c). The overall orientation relations of this structure were determined as:

$$(111)[1\text{-}10]_{STO}||(100)[001]_{TiO2}||(0001)\langle 11\text{-}20\rangle_{GaN} \quad (1)$$

This structure was then used as a template for growing multiferroic $BiFeO_3$ (BFO) by metal organic chemical vapor deposition (MOCVD). While none of the oxides in this structure were single crystalline, and their morphology and orientation are deteriorating with each additional layer – this overall structure still exhibits useful functional properties, as will be discussed in Section 3.2.3 dealing with ferroelectrics on GaN. In a parallel effort to integrate BFO using MBE-grown oxide templates, Yang et al. have scaled the TiO_2 buffer down to 0.6 nm, followed by just 2 nm of (111) STO[73] (Figure 3d) This was followed by MOCVD BFO growth similarly to the previous work.

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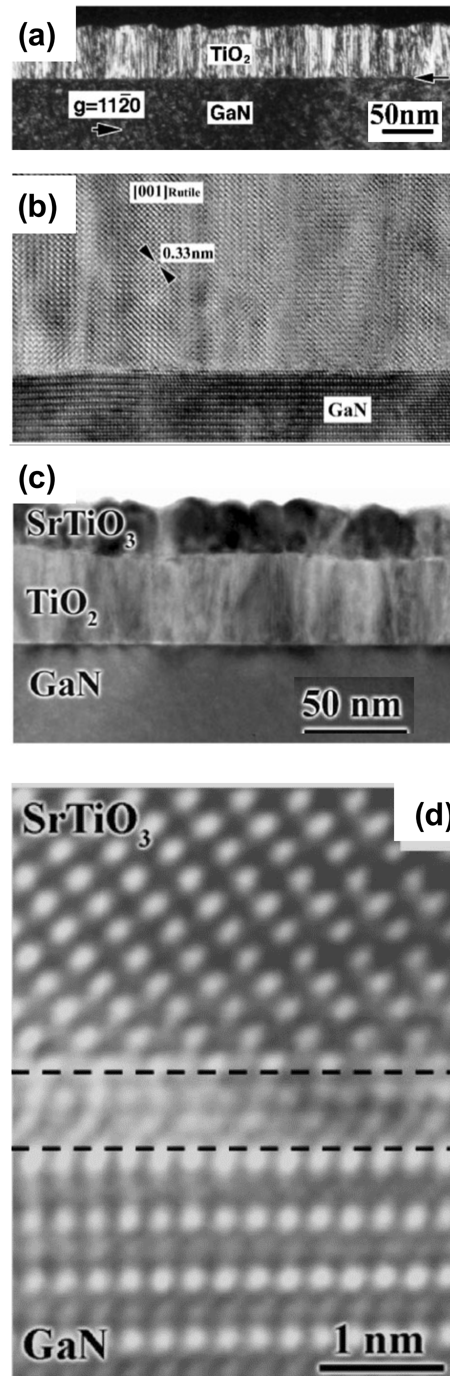

Figure 3. Microstructural properties of oxide/GaN interfaces. TiO_2/GaN interfaces a) at low resolution dark field conditions, showing the various TiO_2 domains in different contrast, and b) at higher resolution showing an atomically-abrupt interface.[14] c) (111) STO grown on top of a TiO_2 buffer,[72] showing 3D features and rough surface, also evident by RHEED (not shown). Despite these structural imperferctions, epitaxial $BiFeO_3$ grown on top of this STO exhibit useful functionality. d) Ultra-scaled templates of ~2 nm STO on 0.6 nm TiO_2.[73] Reproduced with permission.[14,72,73] Copyright 2005, 2007 American Institute of Physics.

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Growth of STO has also been attempted using PLD by Luo et al.,[74] who considered two possible in-plane orientations. In Orientation A $[1\text{-}10]_{STO}\|[1\text{-}100]_{GaN}$ there's a -0.1% mismatch, and in Orientation B the in-plane relations are $[1\text{-}10]_{STO}\|[1\text{-}200]_{GaN}$ with a huge -13.3% mismatch. From an elastic energy perspective, one would have expected orientation B to be completely sidelined by A, as observed with MBE grown films[72] [**Equation (1)**]. However, additional energetic factors, namely chemical energy caused by dangling bonds, may also play a role. And indeed, it was shown that when directly depositing STO on GaN the elastically-unfavorable Orientation B appears to dominate, with strain relaxation occurring via domain formation and 3D growth. The authors therefore used a 2 nm epitaxial layer of TiO_2 to direct the growth into the elastically-favorable Orientation A. This has still resulted in a 3D STO structure, but it was argued to improve the structure, by starting with 2D growth and then transition to 3D (Stranski-Krastanov mode). While the exact mechanisms remain to be clarified, this work nonetheless has further demonstrated the advantage of using TiO_2 as a template for STO epitaxy on GaN, which was already been employed by MBE work.[72,73] It should be noted that the growth kinetics are very different between these two methods.

In summary, it was shown that a rutile-TiO_2 layer facilitates or improves subsequent growth of (111) perovskites on (0001) GaN. No single crystalline oxides were achieved, but well-ordered and textured domain structures were observed, all of which with some 3D morphology. Nonetheless, from a functional point of view, these imperfect-crystallinity templates have facilitated the growth of other oxide over-layers which showed useful functional behavior in devices, as will be described in the following sections.

2.1.7 Chemical Solution Methods

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Chemical solution methods provide a route for low cost and highly scalable epitaxy for a wide range of materials, which can be particularly useful when large thicknesses (>100 nm) are required. One such prominent method is polymer-assisted deposition[75] (PAD). In one example, PAD was used to deposit $BaTiO_3/La_{0.7}Sr_{0.3}MnO_3$ over MBE-grown STO/Si.[76] In another example, Gatabi et al. have used the sol-gel method to deposit $Pb(Zr,Ti)O_3$ over MBE-grown STO/GaAs and STO/Si.[77] Similar work on GaAs was further extended and analyzed by Meunier et al.[60,78] These examples have shown columnar or oriented structures rather than epitaxial growth, and the oxide semiconductor interfaces showed large interface layers. Nonetheless, such properties may be useful for some applications, and indeed, the films in some of these examples have shown some functional properties such as ferroelectricity.

2.2. Physical and Electronic Structure of Semiconductor-Crystalline Oxide Interfaces

Structural interactions at oxide/semiconductor interfaces driven by strain, symmetry mismatch and electrostatic boundary conditions have important implications on device performance. For example, the details of the band offsets are related to the specific atomic-scale structures of the oxide/semiconductor interface and a significant research focus has involved both experimental and theoretical studies of these interfaces. Additionally, defects/dislocations arising from the differences in symmetry of the cubic oxide and diamond/zincblende semiconductor and their potential effects on the physical properties of the oxide/semiconductor system have to be understood. A common defect is the anti-phase boundary observed by high-resolution electron microscopy in $SrTiO_3$/Ge, $SrTiO_3$/Si and $SrZrO_3$/Ge due to the step height mismatch between the semiconductor and the oxide.[12,79]

Initial work focused on understanding the atomic and electronic structure of the STO/Si interface. Due to the high dielectric constants of complex oxides such as $SrTiO_3$ (k=300), their integration with semiconductors as gate dielectrics has been investigated for potentially replacing oxides such as SiO_2 in MOS devices. The gate dielectric is also required to have significant (> 1eV) band offsets[26] with

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the semiconductor for both the conduction and valence band to prevent charge leakage. The details of the band offsets are related to the specific atomic-scale structures of the oxide/semiconductor interface and a strong research focus has involved both experimental and theoretical studies of these interfaces. Other potential functionalities may require low offsets for easy charge transport.[10,80] For the STO/Si interface, spectroscopic measurements show a negligible conduction band offsets for both n and p-type Si[9,81] in agreement with first principles calculations.

Advances in high resolution electron microscopy, synchrotron-based X-ray diffraction measurements which utilize the crystal truncation rod analysis technique, and EXAFS measurements have enabled the atomic-scale characterization of the oxide/semiconductor interface.

2.2.1. Physical Structure of the Semiconductor-Crystalline Oxide Interface

$SrTiO_3$ on Si and Ge: Formation of a Built-in Polarization

A good starting point for understanding the interfacial structure of oxides on Si is based on the growth sequence typically employed experimentally. Zhang and coworkers consider two interfacial structures with either a $Sr_{0.5}O$ layer between the first TiO_2 layer or a full SrO interfacial layer.[82] For both interfaces, a dimerization of the top Si surface is observed giving rise to a 2×1 symmetry. For the full SrO layer, the Sr atoms above the Si dimers are displaced by 0.24 nm in the vertical direction relative to the Sr atoms between the dimer rows. A similar rumpling of the Ba atoms at the dimerized BTO/Ge interface. For both interfaces considered by Zhang et al., a net polarization of the interfacial Sr_xO layer is observed and characterized by a net displacement of the oxygen sublattice relative to the Sr layers by about 0.035 nm. Kolpak et al. compare many possible interfacial structures of STO/Si films and observe an interface dipole characterized by oxygen-cation displacements within the oxide planes adjacent to the interface for all interface structures studies.[83] This work has shown that cation displacement at the first STO layer can vary from 0.010 nm to 0.067 nm, and the conduction band offset can vary from negative 0.2 eV to positive 1.5 eV – as a result of the interfacial atomic structure.

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The theoretically predicted polar structures have been confirmed experimentally by synchrotron diffraction measurements. Aguirre-Tostado and coworkers investigated the STO/Si interface by EXAFS at the Ti K-edge revealing an absence of inversion symmetry of Ti close to the STO/Si interface. This polarization, which decays away from the interface, leads to an anomalous expansion of the STO unit cell for film thicknesses below 10 nm.[84] The polarization at the STO/Si interface was further studied by Kumah et al,[18] using the crystal truncation rod analysis technique and was found to be pinned in agreement with first principles density functional theory predications.[83,85]

Similar polar distortions have been observed on STO and $SrZr_xTi_{1-x}O_3$ (SZTO) interfaces with Ge.[86] Chen and co-workers studied the SZTO/Ge interface as a function of Zr content using synchrotron x-ray surface diffraction and observed a positive polarization in the interfacial oxide layers. The effect of the interface structure on the SZTO/Ge band offset is further investigated theoretically, with calculations showing that the VBO for the polar structures are consistent with photoemission measurements. Conversely, the calculated VBO for structures without polar distortions are found to be ~2 eV less than the polar structures.

$BaTiO_3$ on Ge: Realizing Non-Bulk Structures

The coupling of structural symmetries at the semiconductor-oxide interface can be used to impose local changes in the structure of oxide films to enable new functionality not found in the bulk oxide material. Here we discuss the BTO/(2×1) Ge interface where the 2×1 symmetry of the reconstructed Ge surface stabilizes a BTO structure at the interface whose polarization and band alignment are predicted by first principles calculations to be tunable.

Under growth conditions which favor a stable 2×1 Ge interface, the epitaxial constraint is found to couple to elastic modes in the BTO with a 2×1 symmetry. The atomic structure of a 2.5 unit cell thick 2×1 BTO/Ge interface was studied using a combination of synchrotron X-ray diffraction and first-

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principles density functional theory. The films were grown by MBE. Superstructure reflections were observed for the sample indicative of a 2×1 symmetry of both the interfacial Ge layers and the BTO film which were confirmed by high angle annular dark field imaging. The layer-resolved atomic structure was obtained by analyzing the superstructure reflections and the integer-order crystal truncation rods. The interface comprises of a dimerized Ge layer adjacent to a rumpled 1 monolayer (ML) BaO with displacements of the Ba and O along the BTO [101] direction. The interfacial displacements are found to extend to TiO_2 layer with in-plane Ti displacements found along the [100] direction. Along the [100] direction, a breathing mode distortion is observed with the TiO_6 alternatively contracting and expanding. The observed distortions are not present in the bulk BTO phase diagram and are related to stiff and unstable (soft) elastic modes associated with bulk cubic BTO with a 2×1 symmetry. Force constant matrix eigenmodes dispersion curves were calculated for bulk cubic BTO. The measured distortions relative to the bulk high-symmetry cubic lattice positions were projected onto the static eigenmodes of the force constant matrix. As expected, the largest projections are for soft modes along the X-point, related to anti-parallel Ti and O. The next leading mode is a stiff acoustic mode which involves parallel Ti displacements and anti-parallel O displacements. Zone center displacements results in a non-zero polarization along the x and z directions with an estimated spontaneous ionic polarization of the interfacial BTO determined to be 54 mC/cm^2 which is larger than the bulk room temperature BTO value of 36 mC/cm^2.

The direct relation to the symmetry-stabilized distortions in the oxide film and force constant dispersion matrix which can be obtained from first principles calculations allows for the design of materials with specific structures related to technologically relevant functional properties. For example, breathing mode distortions which are related to charge ordering and metal-insulator transitions, can be stabilized by coupling the surface reconstruction of the semiconductor surface with soft eigenmodes. The 2×1 Zintl interface with ½ ML of the alkaline earth metal can also serve as templates for stabilizing non-bulklike phases in complex oxide thin films.

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Dogan and Ismail-Beigi have performed further theoretical studies of the BTO/Ge interface to investigate the stable phases, interfacial chemistry and the related electronic structures and band alignments.[87] The lowest energy structures with a full interfacial BaO possess either symmetric or asymmetric Ge dimers with the symmetric structure being 0.39 eV per dimer high in energy than the asymmetric structure (**Figure 4**). Breathing mode distortions of the TiO_6 octahedra are found in the asymmetric structures while the TiO_6 octahedra in the symmetric 2×1 structure have identical volume. Two asymmetric structures related by symmetric reflection about the *yz* plane reverses the buckling resulting in the switching of the direction of the in-plane polarization of the BTO. Dynamic switching between the symmetric and the two asymmetric states is desirable since the states possess different spontaneous polarizations and band alignments. For the stoichiometric uncapped films, the energy barrier between the symmetric and asymetric states is computed to be 0.57 eV per cell. A top electrode with a work function of 3.82 eV is found to break the degeneracy of the two states, permitting the non-volatile switching of the polarization by the application of an external bias. Additionally, the band alignment of the asymmetric structure favors holes while the symmetric structure favors electrons, hence, switching between the polarization states simultaneously switches the carrier type of the interface.[87]

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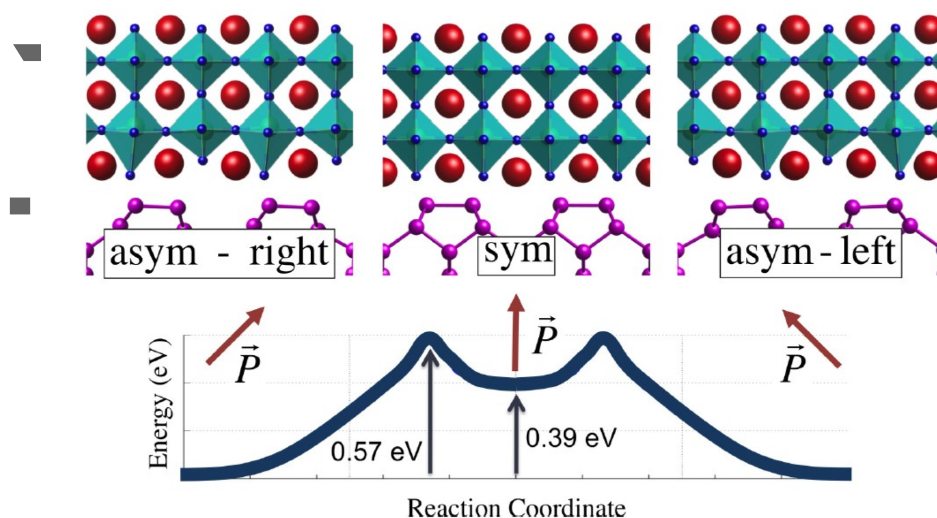

Figure 4. Transition path from the asymmetric structure ("asym - left") to the reflected structure ("asym - right"). The transition passes through the symmetric structure ("sim"), which is a local energy minimum, with barriers of 0.57 and 0.22 eV for entering and leaving this local minimum, respectively. The arrows point at the polarization direction for each structure. The two asymmetric structures feature opposite in-plane polarizations, and identical out-of-plane polarization. Reproduced with permission.[87] Copyright 2017, American Physics Society.

2.2.2. Band Alignments at Semiconductor-Oxide Interfaces

Much progress has been made in understanding and manipulating the band offsets at the oxide/semiconductor interface. For example, coupling of dielectric or ferroelectric polarization to a semiconductor typically requires a type-I (straddling) arrangement, in which the conduction (valence) band of the oxide is above (below) the conduction (valence) band of the semiconductor,[88,89] allowing the oxide to couple as a capacitor. Conversly, for photoelectrocatalysis schemes, a type-II arrangement is desireable.[13] Though epitaxial STO is an excellent platform for the subsequent growth of multifunctional oxides on semiconductors, the type-II band alignment of STO on Si, Ge, and GaAs limits its use as an insulator.[81,90]

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Posadas et al. found that doping STO with Al enhanced the band-gap, which reduces the leakage currents due to the type-II arrangement[91] (staggered). In particular, the band-gap in STO was enhanced by 0.3 eV for Al content between 10-20%, as revealed by photoelectron energy loss and spectroscopic ellipsometry. DFT calculations revealed that Al doping increases the effective band-gap by decreasing the bandwidth of the conduction band. In essence, Al acts as a Ti vacancy that disrupts itinerant hopping between adjacent Ti sites.

Given the limited solubility of Al in STO and relatively modest change in band alignment, another approach to engineer band offsets is to form a solid-solution between $SrZrO_3$ and $SrTiO_3$. This method is most akin to band-gap engineering at III-V heterojunctions, e.g. $Al_xGa_{1-x}As$. The band-gap of $SrZr_xTi_{1-x}O_3$ (SZTO) can be continuously tuned between the band-gaps of $SrTiO_3$ (3.2 eV) and $SrZrO_3$ (5.6 eV) through control of Zr content x. Moghadam et al., demonstrated this approach for epitaxial $SrZr_xTi_{1-x}O_3$ grown on Ge[92] (**Figure 5**). X-ray photoemission spectroscopy (XPS) measurements indicated that a type-I band offset of ~1 eV could be achieved for x=0.7. More importantly, the type-I offset manifests in electrical characteristics of SZTO/Ge gate stacks. The leakage current through the gate stack dropped by as much as ~9 orders of magnitude between x=0 and x=0.7 (Figure 5a). Capacitance-voltage measurements also demonstrated that inversion could be achieved in the x=0.7 heterojunctions on p-type Ge (Figure 5b), which would not be possible if a type-II arrangement were present.

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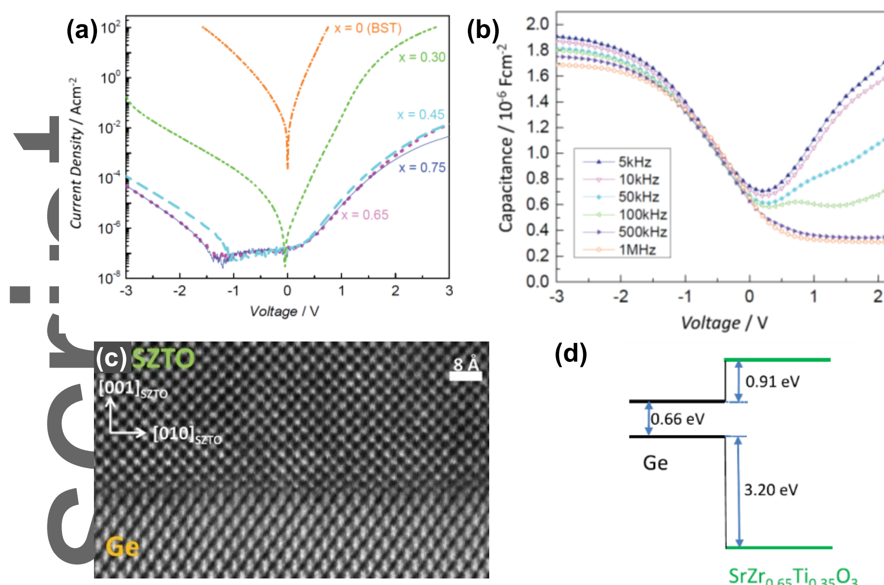

Figure 5. Properties of SZTO/Ge structures. a) Current density versus voltage, showing a dramatic reduction of the leakage currents as a function of Zr content (x), owing to the transition from type-II at low x to type-I at high x. b) Capacitance-voltage analysis of a type-I (x=0.7) structure showing the inversion of the Ge surface at positive voltge. c) Cross section TEM image of the SZTO/Ge interface (x=0.7). d) Type-I band alignment (x=0.65) as measured by XPS. Reproduced with permission.[92] Copyright 2015, Wiley-VCH.

In addition to controlling band-alignment through composition, the interface between crystalline oxides and semiconductors potentially provides another setting in which band alignment could be altered. In contrast to the isostructural interfaces formed at interfaces between conventional semiconductors (e.g. zinc-blende on zinc-blende), semiconductor-crystalline oxide interfaces are heterostructural (e.g., perovskite on diamond-cubic). The interface between the two types of crystal structures in principle allows for some variation in cation and anion composition and configuration that can shift band alignment, according to DFT calculations.[85] We discuss two examples of these studies. Zhang and co-workers compared the 2×1 STO/Si interfacial structures with ½ ML of Sr at the interface and 1 ML Sr at the interface[82] (for both interfaces, a clear 2×1 dimerization of the interfacial Si is observed). For the ½ ML Sr structure, localized states are observed in the interfacial layers which are absent for the 1 ML interface. For the ½ ML interface, conduction band offset and

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valence band offset are 0.87 eV and 1.30 eV respectively, compared with 0.23 eV and 1.9 eV for the 1 ML Sr interface. The calculations of Kolpak et al. predicted that adding oxygen or removing Sr cations at the interface between STO and Si can decrease the valence band offset between the two materials, by effectively modulating the strength of the interface dipole created from bonding.[83] These values are determined from the analysis of the calculated density of states of structurally relaxed 2×1 superlattice slabs. Whether interface structures with variable oxygen and/or Sr content can be experimentally stabilized remains to be seen. If achieved though, engineering the interfacial structure could prove to be a very elegant approach to adjust band-alignment. Preliminary success with this approach is described at the end of Section 3.5.

Experimental studies indicate that oxygen content in the film does affect band alignment. The relation between growth conditions and the interfacial structure on the band offsets have been studied using ultra-violet and x-ray photoemission spectroscopy (XPS). A strong dependence of the interfacial chemistry and post growth treatment on the valence band offsets was found by Amy and coworkers for the STO/p-type (001)Si and BTO/p-type (001)Si interfaces grown with a BaSr silicide with valence band maximum shifts as large as 2 eV.[90] In particular, Amy et al. found that a UV ozone treatment of the oxide surface leads to changes in the reduction in the density of oxygen vacancies and a shift in the oxide band minimum towards the Fermi level. An in-situ anneal at 550 °C in 2×10-5 Torr Oxygen. An upward shift in the STO valence band minimum which is correlated with a change in the oxidization state of the interfacial BaSr silicide buffer layer. SiO_2 formation is observed for vacuum anneals at 650 °C for STO/Si and 550 °C for BTO/Si. The corresponding valence band minimum shifts after the high temperature anneal are on the order of 1 eV compared to the as-received UV ozone cleaned BTO/Si and STO/Si samples.

We conclude this section on band-alignment by discussing developments in x-ray photoemission spectroscopy that not only allow band-alignment to be measured, but also built-in electric fields, e.g. band bending. Prior studies of band alignment at semiconductor-crystalline oxide interfaces were

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performed using conventional XPS, which has a probe depth of only a few nanometers due to the energy of the x-rays generated from a lab source (e.g. Al Kα). Hard x-ray photoelectron spectroscopy (HAXPES) is an emerging technique in which x-rays generated from a synchrotron source are utilized in photoemission studies. The synchrotron x-ray energies typically range from 6 to 8 keV, which allow the probe depth of the photoemission process to be much deeper. Consequently core-level photoelectrons originating from deep below the sample surface or below a buried interface can be measure. Built-in fields manifest as asymmetries in the measured core-level line-shape. The asymmetry arises from cumulative shifts in binding energy that a built-in electric field imposes on photoemitted electrons. By analyzing this asymmetry, built-in electric fields can be quantitatively extracted and spatially mapped across a heterojunction. For example, Du and coworkers utilized HAXPES to quantitatively resolve band bending at a STO/p-Ge interface.[12] They found a space-charge region in the Ge due to electron transfer from the n-$SrTiO_3$. The ability to probe both alignment and built-in fields provides a powerful new tool to understand the electronic structure of semiconductor-crystalline oxide interfaces.

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3. Materials and Functional Properties

In the following section we discuss the various oxide materials that have been epitaxially integrated on semiconductors, and the functional behavior they enable. Such behavior can serve as building-blocks for the development of functional devices and technologies. Our discussion is divided largely along the various classes of oxide materials, namely, insulating dielectrics, ferroelectrics, oxide semiconductors, ferromagnets, superconductors, layered heterostructures, and finally self-organized nanocomposite systems.

Some of the functionalities that we discuss emerge from electrical coupling between the semiconductor and oxide. Examples include MOS, ferroelectric-semiconductor capacitors, oxide semiconductors on conventional semiconductors in which charge transfer and built-in fields are engineered. Other functionalities we discuss stem principally from the oxide alone, in which the semiconductor essentially serves as a physical platform for integration. Examples of the latter include ferromagnetic or strongly correlated oxides integrated on semiconductors, and high temperature superconductors.

3.1. Insulators and High-k Dielectrics

Since the onset of the microelectronics industry, the revolution in information technology has been driven by aggressive scaling of field-effect transistors, which allows more transistors to be fabricated per unit area of the chip. Since the number of transistors per chip is correlated to performance and the chip area is roughly correlated to chip price, we have witnessed an exponential increase in computing power without significant increase in cost for decades.

However, as early as the late 90’s, continued scaling has led to devices in which leakage currents through the nanoscale gate insulator became unacceptably high. At the heart of the problem lies a

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leaky metal oxide semiconductor (MOS) capacitor, which constitutes the gate stack of an MOS field effect transistor (MOSFET), the most basic logic building block.[93] Up to 2007, this capacitor comprised of a degenerately doped polycrystalline Si gate, an amorphous SiO_2 insulator, and doped Si as the channel. The capacitance per unit area (C/A) of the capacitor determines the effectiveness of the switching of the transistor, and is therefore of critical importance to performance.[93,94] Traditionally, as the lateral dimensions of the capacitor have been scaled down, the thickness of the SiO_2 (t_{SiO2}) would be scaled as well.[95] However, as t_{SiO2} reaches nanometric length scales, tunneling gives rise to leakage currents that lead to off-state power consumption and a multitude of performance, stability, and reliability issues. Leakage currents can be minimized by using a thicker gate oxide that is comprised of a material with a higher k, which allows C/A to be maintained despite the higher thickess.[26]

In general, the ideal gate dielectric must meet five key requirements.[26,96] First, the gate material must exhibit a sufficiently high dielectric constant, k, to enable scaling. Second, the oxide must exhibit significant conduction and valence band offsets with the semiconductor to minimize leakage currents (>1 eV). Third, the gate oxide must form a stable interface with the semiconductor. Interfacial layers between the oxide and semiconductor have lower k values and will result in series capacitance that reduces the effective capacitance of the gate stack. Fourth, the interface between the dielectric and semiconductor should exhibit a low density of interface states that trap charge. Such trap states are inevitable at interfaces between amorphous oxides and semiconductors due to the difference in cation coordination, which gives rise to dangling bonds.[6,97] Fifth, the ability to integrate the gate oxide on the semiconductor using scalable, industry-compatible techniques.

In this regard, epitaxial oxides grown on semiconductors can, in principle, satisfy many of these requirements. Epitaxial oxides can exhibit near-ideal abrupt interfaces with the semiconductor, thereby mitigating the formation of an interfacial layer that reduces the overall capacitance. Finally, the ordered placement of atoms associated with epitaxy also minimizes dangling bonds that behave as

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trap states. Given such possibilities, epitaxial oxides have been investigated as candidate gate dielectric materials for Si, Ge and GaN. We review these efforts below.

3.1.1. Insulating Epitaxial Oxides on Si

The first demonstration of an epitaxial oxide on a semiconductor, $SrTiO_3$/Si, was proposed as a high-k dielectric as early as 1998, in the pioneering work of McKee et al.[1,3] (Figure 1a). A capacitance-equivalent of lower than 1 nm of SiO_2 was demonstrated, using a 15 nm thick $SrTiO_3$ (STO) film.

Merely eleven months after the publication of the seminal STO/Si paper.[1] Eisenbeiser and co-workers from Motorola have realized transistors based on epitaxial STO/Si.[98] Using an 11 nm epitaxial STO layer, they obtained an equivalent SiO_2 thickness of 1.0 nm, which included a ~0.7 nm thick amorphous layer at the interface (**Figure 6a**). This lower-k interface layer dominated the capacitance. Both n- and p-MOSFETs with 1.2 µm channel length were demonstrated, showing nominal transistor transfer characteristics (Figure 6b). These devices exhibited subthreshold slopes on the order of ~100 mV/decade. However, due to the type-II band arrangement between STO and Si, high leakage currents of 3-140 mA/cm^2 at a gate voltage of ±1 V were reported. $LaAlO_3$ with a bandgap of 5.4 eV, grown on ultra-thin STO/Si was considered as a possible solution for reducing leakage currents.[99,100]

Using another oxide with a larger band-gap, Rossel and co-workers from IBM demonstrated working transistors based on ~4 nm epitaxial MBE-grown $SrHfO_3$ (SHO).[101] SHO has a bandgap of ~6.5 eV, about twice of that for STO, with high band offsets of 3.1 and 2.1 eV holes and electrons, respectively. Though the band offsets are favorable, SHO has a large lattice mismatch of ~6% relative to Si, which results in mosaic oriented structure, as evidenced by a 4° rocking curve width around the (002) reflection of the oxide. TEM and XPS confirm the presence of an interface layer, which the authors estimate to be ~9A (Figure 6c). Nonetheless, the authors report an effective capacitance equivalent of 0.69 nm SiO_2, which is among the lowest reported for transistors, even to this day with

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ultra-scaled high-k technology. Table 2 shortly compares some of the transistor performance (Figure 6d) to the previous work, showing dramatic improvement in the performance as a capacitor (first three lines of the table), versus considerable shortfalls in the performance as a transistor (last three lines). The authors point out that some of these low performance characteristics are generic to ultra-scaled devices, and don't indicate specific problems the SHO/Si structure.

Despite the progress made in integrating epitaxial high-k oxides on Si, the challenges appear to exceed the benefits, particularly in comparison to the integration of amorphous HfO_2, which has been successfully implemented by industry. However, the transition from Si towards Ge and interest in finding dielectrics for GaN may open new opportunities for epitaxial oxide gate dielectrics.

Table 2. Comparison of the performance characteristics of transistor examples based on epitaxial oxide insulators.

	Motorola[98] 2000	IBM[101] 2006
Material	$SrTiO_3$/Si	$SrHfO_3$/Si
Physical thickness (nm)	11	4
Equivalent capacitance SiO_2 thickness (nm)	1.0	0.69
Range of gate leakage currents at V_g=+1, -1 V (mA/cm^2)	3-140	< 2
Subthreshold slope (mV/decade) (for 10 µm channels)	95-103	307-365
Electron mobility (cm^{2}V^{-1}s^{-1})	221	7.5-28
Hole mobility (cm^{2}V^{-1}s^{-1})	62	2.4-59

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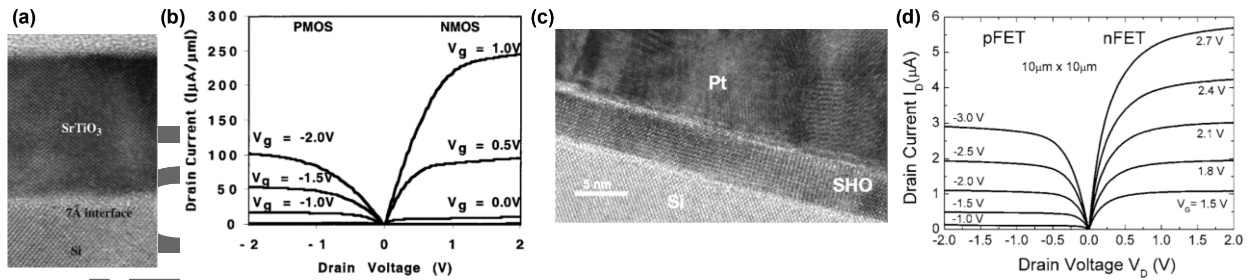

Figure 6. Field effect transistors fabricated using epitaxial oxides as a high-k gate insulator on Si.The first such transistor based on STO/Si[98] (a) Cross sectional TEM micrograph showing a ~0.7 nm amorphous low-k interface layer below nominally 11 nm STO, resulting in a total capacitance effective SiO_2 thickness of 1.0 nm, which is dominated by the interface layer. (b) Transfer characteristics of p- and n-MOSFET transistors with an effective channel length of 1.2 μm. In comparison, the (c) Microstructure and (d) Transfer characteristics of a more advanced generation[101] based on SHO/Si. Table 2 compares the performance of the devices. Reproduced with permission.[98,101] Copyright 2000, 2006, Amerian Institute of Physics.

3.1.2. Insulating Epitaxial Oxides on Ge

Si technology is gradually transitioning to $Si_{1-x}Ge_x$ with increasing x,[102] and to all-Ge channels, owing to the superior mobility of Ge for both electrons and holes. The epitaxial oxide/Ge interface is more thermally stable than its Si counterpart, owing to the lower tendency of Ge to oxidize and reduce the epitaxial oxide. This makes Ge a more feasible candidate for epitaxial high-k oxides compared to Si, though several challenges remain. The conduction band of STO (BTO) is below (aligned with) the conduction band of Ge.[11,12] The absence of a barrier for electron transport facilitates some applications[80] (e.g. Section 4.4), but is detrimental for gate insulators.

To increase the conduction band offsets, Jahangir-Moghadam et al. alloyed the B-site Ti cations with Zr, forming the solid-solution $SrTi_{1-z}Zr_xO_3$, or SZTO.[92] This work was subsequently extended to x=1, or $SrZrO_3$, SZO.[103] The addition of Zr to STO is known to increase the bandgap[104] up to 5.6 eV for x=1, which also raises the conduction band of the oxide above the conduction band of Ge, forming a barrier for electron transport. X-ray photoemission spectroscopy determined that the conduction band

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offset is 0.91 eV for x=0.65, and current-voltage measurements showed a decrease in leakage currents by as much as 7 orders of magnitude from x = 0 to x = 0.65. A relative dielectric constant of ~29 was obtained from capacitance analysis, which is higher than HfO_2. In the follow up work with x=1, despite a larger barrier of 1.4 eV for electrons, the leakage currents were not improved by much (since the layer was about 1/4 of the thickness in the original work, this comparison is based on currents under the same electric field rather than the same voltage). The larger lattice mismatch between Ge and SZO likely results in a greater number of defects, which may also contribute to greater current leakage.

Another important thrust towards epitaxial insulating high-k oxides on Ge has been led by McDaniel et al. in their pioneering work of growing epitaxial STO on Ge exclusively using ALD[30] (Section 2.1.2). Impressively, no oxidized Ge has been detected by XPS, which is critical for preserving high capacitance density. However, preventing the oxidation of Ge during and after growth requires strict limits on the oxygen pressure; this results in oxygen vacancies in the film that enhance conductivity through n-type doping (see discussion in Section 3.5). This trade-off is likely a key contributor to leakage current. Beyond oxygen vacancies, the absence of barriers for electron transport at the STO/Ge interface also contributes to leakage currents. However, the authors showed that by alloying Al (to substitute Ti, ≤18%) these leakage currents can be reduced.

In a follow-up work, McDaniel et al. used ALD to grow crystalline $SrHfO_3$ (SHO) on Ge, which similar to SZO, features a larger bandgap and lattice constant.[31] The authors measured a conduction band offset of ~2.2 eV with XPS, which is the largest reported to date with epitaxial oxides on Ge, and a relative permittivity of ~18. Likely due to the oxygen deficiency described in the previous paragraph, the leakage currents through a 4 nm SHO/Ge structure remained high. Attempts to further reduce leakage by oxygen anneals provided some success, but at the cost of degradation of the SHO/Ge interface quality, manifested by an increase in the density of interface states and a small reduction of the total capacitance. More progress was made in this and in a follow up work[105] with

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bilayer insulators. This was done by employing an overlayer of amorphous Al_2O_3 grown by ALD[106] on top of crystalline SHO/Ge. Careful analysis of the electrical properties have resulted in considerable reduction of the leakage currents. The lowest leakage was shown to be with 2 nm Al_2O_3 over 4 nm SHO/Ge, on the order of 10^{-7} A/cm^2 at a ±1 V range, while maintaining a capacitance density of 1.6 μF/cm^2. For comparison, the same structure without the 2 nm Al_2O_3 layer showed almost twofold higher capacitance density, but at the cost of leakage currents that were more than three orders of magnitude higher at ±1 V. Altogether this effort has shown considerable improvement in the properties of these materials to the point where they are useful for device purposes, and most importantly, this was achieved using ALD, a scalable, microelectronics-compatible growth method.

3.1.3. Insulating oxides on GaN

Several epitaxial oxides have been grown on GaN, with the aim of forming an epitaxial high-k dielectric insulator. Some examples are listed in Table 3. As described in Section 3.1, ordered epitaxial interfaces are attractive for their potential to inimize dangling bonds that act as interface trap states. Many GaN devices are based on AlGaN-GaN 2DEG as a channel, where AlGaN also serves as the insulator. However, it was shown that growth of an additional insulating layer on top further reduces gate leakage currents, and may further improve device performance by passivating states at the AlGaN surface.

Previous works have looked at a wide range of epitaxial oxides, of various crystal structures and compositions as high-k insulators on GaN, using MBE, PLD and ALD, with some prominent examples listed in Table 3. We note MBE-grown hexagonal Gd_2O_3 [69] and monoclinic PLD-grown perovskite $GdScO_3$ [107] are top performers, obtaining leakage currents on the order of μA/cm^2 at 1.5 MV/cm, and permittivities of ~24.

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Table 3. Parameters of some epitaxial insulating oxides grown on GaN

Oxide	Structure	Growth method	k	Eg (eV)	VBO, CBO& (eV)	Leakage
TiO_2 [14]	rutile (tetragonal)	MBE	70	3.0#	0.05, 0.38	AlGaN in series
Gd_2O_3 [69]	hexagonal	MBE	24	5.4	0.55, 1.45	<10 μA/cm^2 @1.5 MV/cm
Gd_2O_3 [108]	hexagonal	PLD	12~14	5.9#	1.8, 1.7	~5 mA/cm^2 @1.0 MV/cm
Y_2O_3 [70]	monoclinic	MBE	20			3.3 μA/cm^2 @1.5 MV/cm
$LaLuO_3$ [71]	hexagonal	PLD	26	5.2		Not insulating, GaN pinholes
Er_2O_3 [109]	bixbyite (cubic)	ALD		5.3#	0.7, 1.2	
$GdScO_3$ [107]	perovskite (cubic)	PLD	24#	5.3	3.7, (-1.7)	~0.2 μA/cm^2 @1.5 MV/cm ~0.2 mA/cm^2 @5 MV/cm

#Values taken from the literature and not measured directly

&Valence and conduction band offsets, respectively. Positive values indicate a barrier for electrons (CBO) and holes (VBO) for crossing from the semiconductor into the oxide.

In one of the first papers on oxide/GaN epitaxy, Hansen et al. have also taken this structure to the next level by demonstrating a functional device.[14] A heterojunction field effect transistor (HFET) was fabricated from 50 nm epitaxial TiO_2 (Table 3) grown over AlGaN-GaN, in which the 2DEG in the GaN served as the channel. This work compared similar devices with and without TiO_2. The authors observed a 10~20% reduction of the saturation currents, likely due to the lower capacitance caused by the addition of the oxide layer in series, which also manifested by a slight degradation of the

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subthreshold slope. However, at the cost of this slight decrease in performance, the TiO_2 layer reduced leakage currents by four orders of magnitude, across gate voltages exceeding 40 V.

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3.2. Ferroelectrics

Ferroelectrics integrated on semiconductors have long been proposed to serve as a platform for the development of computing and sensing devices. For such proposed devices, the ferroelectric functions as a gate material in which its reorientable polarization manipulates carriers in a semiconducting channel. For applications in sensing, ferroelectric gate materials could lead to field-effect devices that are sensitive to temperature and pressure.[110] For computing, ferroelectrics on semiconductors could lead to nonvolatile field-effect devices for logic and memory due to the presence of a remnant, switchable polarization. More recently, it has been proposed that ferroelectric gate materials could produce a negative capacitance effect that enables field-effect transistors to exhibit a sub-threshold slope that is < 60 mV/dec[111,112], which is currently a physical limit in current semiconductor technology.[93] In essence, a ferroelectric gate can momentarily amplify an applied gate voltage, since a switching polarization is driven in part by energy stored in the material, as opposed to being strictly a conventional linear response to an applied field. To maximize the negative capacitance effect, a single crystalline ferroelectric gate with a single domain is needed.

Integrating single-crystalline ferroelectrics on semiconductors in which the polarization of the former is coupled to carriers in the latter is non-trivial,[113] as a variety of material related challenges need to be overcome. Such challenges arise from a mismatch in lattice constants, differences in thermal expansion between the semiconductor and epitaxial ferroelectric, and a type-II band arrangement between the oxide and semiconductor.[114] We discuss each of these challenges and efforts to overcome them below.

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This section will start with ferroelectrics integration on Si and Ge, which are by far the most studied examples. The discussion will then be extended to GaAs and GaN in two subsequent subsections.

3.2.1. Ferroelectrics on Si and Ge

Efforts to integrate single crystalline ferroelectrics on semiconductors have focused largely on the archetype materials $BaTiO_3$ (BTO) and Si. In bulk, ferroelectric BTO exhibits a polarization of 26 μC/cm^2. The paraelectric to ferroelectric transition occurs at T_C=130 °C, which is accompanied by a change in the lattice from cubic to tetragonal symmetry. The in-plane lattice constant of ferroelectric BTO is 3.99 Å, which is nearly 4% larger than the Si (100) surface lattice constant of 3.84 Å. Due to this mismatch, epitaxial BTO films on Si rapidly relax with increasing film thickness. The rapid relaxation with thickness is further enhanced by steps on the surface of (100) oriented Si substrates. Such steps arise from an unavoidable residual miscut in the substrate, and are incommensurate with respect to the BTO unit-cell in the growth direction. Relaxed films, however, can experience tensile strain as the film is cooled from growth to room temperatures, due to the large difference in thermal expansion between BTO and Si. Tensile strain gives rise to BTO films with an in-plane polarization, which is not useful for devices in which the polarization is to be coupled to carriers in the semiconducting electrode. To mitigate the effects of film relaxation and differences in thermal expansion, Vaithynathan et al. utilized a fully relaxed 30 nm thick buffer layer of $Ba_{0.7}Sr_{0.3}TiO_3$ between a 10 nm thick BTO top layer and Si.[115] When relaxed on Si, this buffer layer, which has a smaller in-plane lattice constant than the BTO, imparts compressive strain, thereby overcoming the tensile strain from the Si. A switchable out-of-plane polarization in the BTO layer was measured through piezo-response force microscopy (PFM).

This approach of utilizing a buffer layer to impart compressive strain has been employed in subsequent studies. Dubourdieu et al. used a layer of $SrTiO_3$ as a buffer and demonstrated that BTO

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films exhibiting an out-of-plane polarization could be achieved on Si for film thicknesses ranging in thickness from 8 to 40 nm.[116] In their study, a layer of SiO_2 formed between the STO/BTO stack and the doped Si. Interestingly, ferroelectricity in the BTO films, as inferred through PFM, was stable even in the presence of the SiO_2 and absence of a conducting bottom electrode. Hsu et al. and Merckling et al. have further addressed this challenge with a systematic structural investigation of the relaxation of STO buffer layers on Si and its effect on the orientation of the overlaying BTO.[117,118] Similarly, Ngai et al. used a compositionally graded buffer layer comprised of $Ba_{1-x}Sr_xTiO_3$ to realize thick BTO films (40-60 nm) on Ge,[119] showing ~0.5 V hysteresis in current-voltage analysis of this structure. By tuning the Sr content x throughout the graded buffer, compressive strain could be controlled as manifested in a tunable out-of-plane lattice constant of the BTO films grown on top.[88] Ponath et al. utilized a thin buffer layer of $SrTiO_3$ to realize 15 nm thick, c-axis oriented BTO films also on Ge.[120] Aside from the use of piezo-force microscopy (PFM), this latter study also demonstrated coupling of the ferroelectric polarization to carriers in Ge through microwave impedance spectroscopy. The retention time of the polarization of such films on Ge is promising.[120]

However, for potential applications in CMOS, aggressive lateral scaling of transistors places constraints on the overall thickness of a ferroelectric gate stack.[121,122] In general, ferroelectricity is weakened with decreasing film thickness, as the effects of depolarization fields are enhanced.[114] Aside from increasing the thickness of a gate stack, non-ferroelectric buffer layers can also enhance the effects of depolarization fields; thus, pathways to realize very thin ferroelectric gate stacks on semiconductors are also needed. One approach is to induce ferroelectricity in the buffer layer itself, thereby eliminating the need for an additional ferroelectric layer grown on top. In this regard, stoichiometric $SrTiO_3$ (STO) is predicted to exhibit ferroelectricity at room temperature under compressive strain.[123,124] Indeed, Waruswithsana et al. found that ultra-thin films of STO under epitaxial compressive strain on Si exhibit switchable contrast in the amplitude response of the PFM signal, consistent with ferroelectricity.[124]

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Another route to inducing ferroelectricity in ultra-thin layers of STO is to introduce Sr vacancies, which create weakly interacting polarized clusters known as polar nano-regions (PNRs). PNR's are a defining feature of relaxor ferroelectrics.[125] For some relaxor materials, a true ferroelectric state defined by the development of long-range polarization can emerge as a function of temperature or applied field.[126] For Sr deficient STO films grown on metallic electrodes, a ferroelectric state can indeed be induced, even in the absence of compressive epitaxial strain, as demonstrated by Lee et al.[127] It should be noted that even in the absence of a true ferroelectric state, applied-fields can re-orient PNRs to induce macroscale polarization that persists for long periods of time, as found in so-called canonical relaxors. In principle, a persistent polarization in a relaxor could provide essentially the same functionality that a remnant polarization provides in a conventional ferroelectric.

Aside from enlarging the palette of candidate gate materials, the use of relaxors can also address another key challenge, namely, the type-II band alignment between conventional ferroelectrics, such as BTO, and semiconductors such as Si, Ge, and GaAs. Thus far, the studies of ferroelectric-semiconductor heterojunctions discussed above have inferred the presence of ferroelectricity predominantly through PFM. Ideally, direct measurement of the polarization as a function of applied field (e.g. P-E measurements) would not only enable the hysteretic polarization to be quantified, but also fully establish a ferroelectric state through observation of saturation in the polarization. Such measurements are challenging for metal-ferroelectric-semiconductor gate stacks due to the type-II band alignment between BTO and Si, Ge, etc., which give rise to leakage currents. For example, a type-II band alignment produces hysteretic diode-like behavior in the vertical electrical transport characteristics of Pt/BTO/$Ba_{1-x}Sr_xTiO_3$/Ge gate stacks.[119] One approach to mitigate the type-II band alignment is to insert a buffer layer that has a type-I arrangement between the ferroelectric and semiconductor, as was demonstrated by Murphy et al. for BTO grown on MgO buffered GaAs.[128] Another approach is to use relaxor materials that have a type-I band offset with respect to the semiconductor, as demonstrated by Moghadam et al. in their study of $SrZr_{0.7}Ti_{0.3}O_3$ (SZTO) on Ge.[129]

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A switchable persistent polarization could be induced through applied fields, as indicate in both amplitude and phase response of PFM and piezo-response spectroscopy measurements. The type-I band offset enabled measurement of the hysteretic component of the polarization, through polarization-electric field measurements in the so-called positive-up negative-down (PUND) configuration. Most encouraging, the SZTO layer could modulate the surface potential of Ge, as demonstrated through capacitance-voltage measurements for films as thin as 5 nm.

We conclude this section by discussing how the interface can be exploited to achieve ferroelectric functionality in a semiconductor-oxide heterojunction. While buffer layers, compressive strain and the use of relaxor materials address key challenges associated with realizing functional single-crystalline ferroelectric-semiconductor heterojunctions, functionalizing the interface between an oxide and (100) surface of Si provides an alternative and perhaps more elegant pathway. In general, the semiconductor-oxide interface presents both challenges and opportunities to realizing a ferroelectric-semiconductor heterojunction. As discussed in prior sections, bonding between a STO and Si, or $SrZr_xTi_{1-x}O_3$ and Ge yields a polarization that is pinned and upward oriented. Kolpak et al. found that this fixed polarization was germane to a variety of interfacial compositions that mediate epitaxy between STO and Si.[85] Such a fixed polarization inhibits switching of a ferroelectric layer, unless disrupted through the formation of a native Si or Ge oxide layer.[129] However, bonding at the (100) surface also presents an opportunity. Dogan et al. predicted that a single monolayer of ZrO_2 on the Si(100) surface exhibits bi-stable polarization states, thereby providing the same functionality as a conventional ferroelectric.[130] The polarization emerges from rumpling of the ZrO_2 planes, which are normally unswitchable in bulk specimens due an energy barrier that scales with size. However, switching in a single monolayer thick ZrO_2 layer is energetically possible. The authors experimentally demonstrated the viability of a single monolayer ZrO_2 ferroelectric, as capacitance-voltage measurements showed hysteretic modulation of the surface potential of Si by ~0.4 V. Aside from allowing very aggressive scaling of devices, the single monolayer ZrO_2 ferroelectric also simplifies

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the fabrication of the gate stack, as a conventional dielectric, such as amorphous Al_2O_3, can be utilized to switch the ZrO_2 at the interface while reducing leakage currents.

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3.2.2. Ferroelectrics on GaAs

The first to overcome the challenges of integrating ferroelectrics with GaAs was Contreras-Guerrero et al.[52,131] In their pioneering work they demonstrated high quality BTO layers on GaAs (**Figure 7a,b**), using the dual-chamber growth technique described in Section 2.1.5. This was achieved using a template of 2 unit cells of STO, obtained using the 1/2 ML Ti approach for passivating the GaAs surface.[63] For these structures, piezoresponse force microscopy (PFM) revealed a coercive voltage of 1-2 V and a piezoresponse amplitude of ~5 pm/V (Figure 7c-g).

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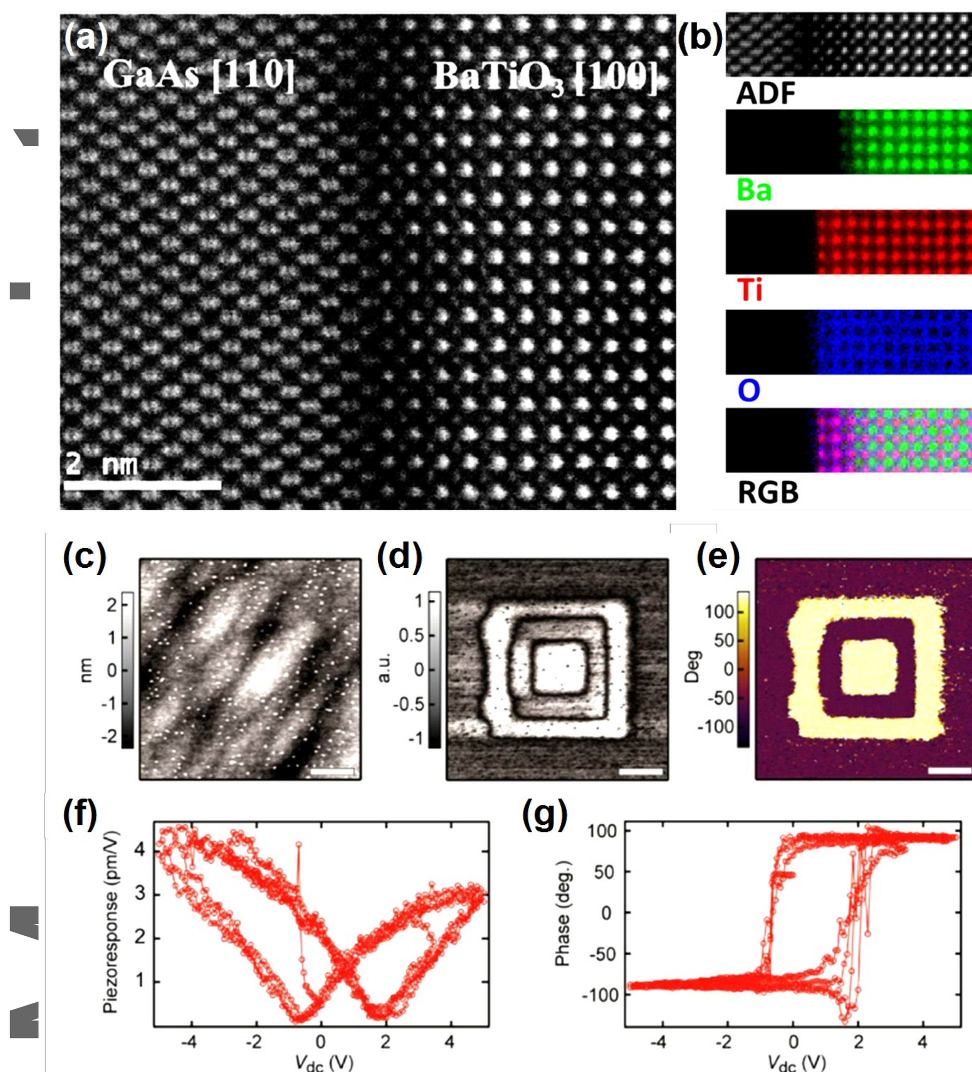

Figure 7. Structure and functioality of ferroelectrics integrated on GaAs. 8 nm ferroelectric BTO was grown on 2 unit cells STO-templated GaAs. a) General view of the interface. The first two atomic layers in the oxide ($SrTiO_3$) can be seen to be a lower intensity, owing to the lower atomic mass of Sr versus Ba. Reproduced with permission.[131] Copyright 2013, Elsevier. b) Atomic-resolution electron energy loss spectroscopy (EELS) mapping of the elements in this interface. Reproduced with permission.[57] Copyright 2015, Amerian Institute of Physics.

Ferroelectric characterization using PFM, showing (c) topography, (d) PFM amplitude and (e) PFM phase (V_{ac}=0.5 V, scale bars are 1 μm, 3×3 μm^2 features were patterned with V_{dc}=3 V). (f) Amplitude and (g) phase curves (V_{ac}=4 V). Reproduced with permission.[52] Copyright 2013, Amerian Institute of Physics.

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Aside from BTO, ferroelectric PZT has also been integrated on GaAs. Louahadj et al. first grew a 8 nm thick buffer layer of STO on GaAs using MBE, with an initial 1/2 ML Ti passivation layer.[132] The sample was then transferred *ex-situ* to a PLD chamber, where a bottom 30 nm electrode of conductive $La_{1-x}Sr_xMnO_3$ (LSMO, see Section 3.4.2) was grown, followed by 100 nm of PZT. Ferroelectricity was confirmed by PFM performed on the film surface. In addition, interdigitated Pd electrodes were used to further explore ferroelectricity, showing a memory window of ~1.1 V; yet, this observation did not show scalability with the electrode surface. This was interpreted by the authors as evidence that the dielectric response originates by the vertical fields running between the fingers through PZT, thus being generated by domains oriented in the out of plane direction. We note that unlike MBE grown BTO/STO on GaAs,[52,131] the use of a bottom LSMO electrode decouples the ferroelectric PZT from GaAs. Furthermore, the PLD growth conditions of LSMO and PZT (including 300 Torr O_2 at 600°C for 10 min) likely altered the GaAs. Nonetheless, this work presents new concepts and routes towards potentially efficient ferroelectric integration on GaAs.

3.2.3. Ferroic Oxides on GaN

Combining oxides that possess properties such as ferroelectricity and magnetism with GaN provides attractive prospects of novel functional devices. Posadas et al. have used off-axis RF magnetron sputtering to grow multiferroic hexagonal $YMnO_3$ directly on GaN,[133] where ferroelectricity and antiferromagnetism coexist and are weakly coupled.[134,135] Interestingly, despite a 4% lattice mismatch between $YMnO_3$ and GaN, a 30° in-plane rotation of the $YMnO_3$ unit-cell was observed that results in ~10% lattice mismatch. First principle calculations have shown that this rotation is driven by energetically favorable chemical bonding at the interface, which overcomes the cost in energy associated with strain. Similar behavior was observed for PLD-grown rutile TiO_2 on GaN (Section 2.1.6). Both ferroelectric (Figure 8a) and antiferromagnetic behaviors were observed on GaN.[133]

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In contrast to the direct integration of $YMnO_3$ on GaN, Yang et al. employed an ultra-thin STO (111)/TiO_2(100) template layer grown by MBE, upon which multiferroic rhombohedral $BiFeO_3$ films were grown using MOCVD (see Section 2.1.6 for more information on the template). Metal-oxide semiconductor (MOS) capacitors were subsequently formed by evaporating Pt pads on this structure. The ferroelectricity of $BiFeO_3$, with an out-of-plane (pseudocubic) <111> easy axis was probed using capacitance-voltage (C-V) analysis of these MOS devices[72] (Figure 8b). See Section 2.1.6 for further details on the growth of this specific system.

Another successful ferroelectric integration with GaN using STO/TiO_2 buffer layers conducted by Luo et al.,[136] who employed PLD to deposit ferroelectric Hf-doped $Bi_4Ti_3O_{12}$ (BTH, Table 4). This ferroelectric was deposited on a conductive $SrRuO_3$ electrode, forming a capacitor that is not electrically coupled to the semiconductor. In addition to a thorough investigation of the structure, this work further addresses important practical aspects of ferroelectric behavior, including material fatigue (exhibiting 10.2% degradation after 1.1×10^{10} cycles), and leakage (<2 $\mu A/cm^2$). Alternative integration approaches were attempted by PLD[137] and RF magnetron sputtering[138] of ferroelectric $Ba_{0.5}Sr_{0.5}TiO_3$ directly on GaN without buffer layers, which resulted in films that exhibited domain structures.

More recently, Elibol et al.[139] employed thick (tens of nm) rutile TiO_2 layers as templates for the growth of ferroelectric $Pb(Zr_{0.52}Ti_{0.48})O_3$ (PZT) using PLD, which yielded films with an in-plane polarization. A follow-up work by this group[140] replaced the thick TiO_2 buffer layer with MgO, which also yielded ferroelectric films with an in-plane polarization (Figure 8c).

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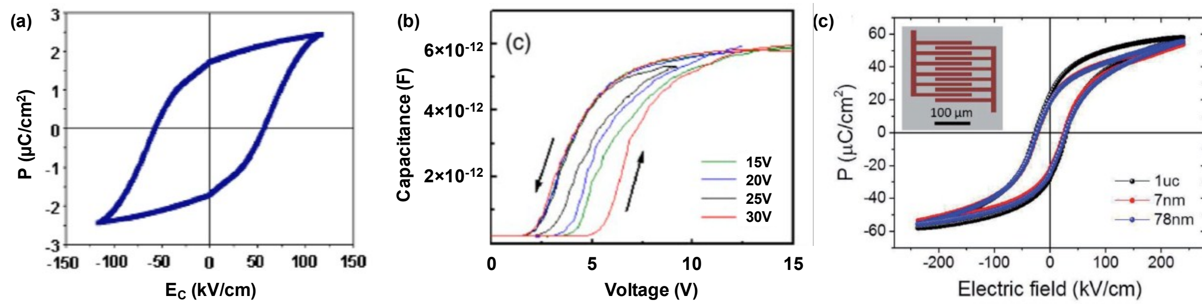

Figure 8. Ferroelectric behavior of oxides on GaN. a) Out of plane polarization – electrical field (P-E) loop of multiferroic $YMnO_3$/GaN. Reproduced with permission.[133] Copyright 2005, Amerian Institute of Physics. b) Hysteretic Capacitance – voltage (C-V) curves of $BiFeO_3$/STO/GaN MOS structures. Reproduced with permission.[73] Copyright 2007, Amerian Institute of Physics. c) In-plane P-E loops of PZT/MgO/GaN structures, where the different curves represent different MgO buffer thicknesses. Reproduced with permission.[140] Copyright 2018, Wiley-VCH.

Table 4. Summary of some of the reported ferroelectric/GaN properties. It is noted here that the ferroelectric performance considerably depends on process details and interface structure; thus the properties of known ferroelectrics may vary considerably when grown on semiconductors.

Material	Buffer	Growth	Ferroelectric Thickness (nm)	Geometry	Remnant polarization ($\mu C/cm^2$)	Coercive field (MV/cm)	Ref.
$Ba_{0.5}Sr_{0.5}TiO_3$ [137]	none	PLD	600	out-of-plane (MOS)			Cho '04
$YMnO_3$ [133]	none	sputtering	40-400	in-plane	2	50	Posadas '05
$BiFeO_3$ [73]	MBE STO(TiO_2)	MOCVD	300	out-of-plane (MOS)			Yang '07
BTH [136]	$SrRuO_3$/ STO(TiO_2)	PLD	400	out-of-plane (capacitor)	~23	~150	Luo '09

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PZT [139]	TiO2	PLD	300	in-plane	25.6		Elibol '15
PZT [140]	MgO	PLD	750	in-plane	~20	~26	Li '18

3.3. Semiconducting Oxides

Semiconducting oxides integrated on conventional semiconductors provide a setting in which charge transfer and built-in electric fields can be engineered across the interface. Charge transfer and built-in fields across heterojunctions between conventional semiconductors underpin the functionality of virtually all semiconductor-based technologies. For example, the built-in electric field of a pn-junction underpins the functionality of solar-cells and the ubiquitous field-effect transistors that have revolutionized computing. In principle, the atomically abrupt interfaces that can be achieved at semiconductor-crystalline oxide interfaces using MBE enable continuity in the electric displacement, which is essential for charge transfer and built-in fields to form. Engineering charge transfer and built-in fields could lead to hybrid semiconductor-oxide pn-junctions, isotype n-n junctions or intrinsic-doped heterojunctions that could be utilized in applications ranging from photocatalysis to nanophotonics.

Charge transfer and built-in fields have recently been explored in heterojunctions between STO and Ge and Si. As discussed in Section 2, recent developments in HAXPES have opened pathways to quantify and map built-in electric fields across semiconductor-oxide heterojunctions.[141] Du et al. initially demonstrated this approach to map band-bending in p-type Ge at a heterojunction with epitaxial STO.[12] A more dramatic example of built-in fields was recently demonstrated by Lim et al. in their study of heterojunctions between $SrNb_xTi_{1-x}O_3$ and Si.[142] The built-in field was sufficiently strong to induce the formation of a hole-gas near room temperature in the Si. By tuning the carrier density in the oxide layer via the Nb content, the authors were able to tune the sheet density of the

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hole-gas in Si. Employing the HAXPES techniques described above, the authors were also able to map out the built-in fields in both the $SrNb_xTi_{1-x}O_3$ and the Si. These results represent key progress in the development of semiconductor-oxide pn-junctions, n-n junctions, etc.

While band-gap engineering and charge transfer through control of carrier density have been separately demonstrated, combining the two techniques in a single heterojunction will allow control akin to that which can be achieved in heterojunctions between III-V semiconductors.[143] The large conduction band offsets, large dielectric constants could lead to electron-gases at semiconductor-crystalline oxide interfaces that exhibit extremely high carrier densities and also high mobilities. In light of the high mobilities of conventional semiconductors that give rise to low carrier scattering, such extreme density electron gases could serve as a platform for plasmonic/nanophotonic devices.

3.4. Ferromagnetic Oxides and Strongly-Correlated Metals

Ferromagnetic oxides and strongly correlated metals exhibit behaviors that are fundamentally fascinating and also technologically important. For example, the field of spintronics constitutes an active research area for physicists and engineers,[144,145] and its potential for coupling with conventional electronics is highly attractive. In particular, ferromagnetic oxides that exhibit high spin polarization, such as $La_{1-x}Sr_xMnO_3$ (LSMO), could provide a platform for spintronic and opto-spintronic applications if integrated on semiconductors. While the examples discussed below have yet to demonstrate spin-injection via the ferromagnetic oxide, their integration on semiconductors is an important first step (Figure 9, Table 5).

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Table 5. A summary of conductive materials that can be integrated with semiconductors, their properties, functionalities and potential applications.

Material	**Key properties and functionalities**	**Potential applications**
$SrRuO_3$ (SRO)[146]	conductor, ferromagnetic (<150 K), magnetocrystalline anisotropy	conductive electrode, e.g. back electrode for ferroelectric devices
YBCO [147]	high temperature superconductor	superconducting electronics, communications and computing
$La_{1-x}Sr_xMnO_3$ (LSMO) [148,149]	double-exchange ferromagnetism, colossal magnetoresistance (CMR), metal insulator transitions	MEMS devices Magnetic sensors Spintronic devices Mottronics and field effect devices Conductive back electrode for ferroelectric devices
Oxide 2DEGs: $LaAlO_3$/STO [150] $LaTiO_3$/STO [10,151] $GdTiO_3$/STO [152,153] $LaTiO_3$/STO/Ge [154] $GdTiO_3$/STO/GaAs [55]	high density (10^{13}-10^{15} cm^{-2}) of confined, correlated electrons very low temperature superconductivity (<0.2 K)	Chemical sensors Spintronic devices Sketched nanoelectronics Channels for field effect devices

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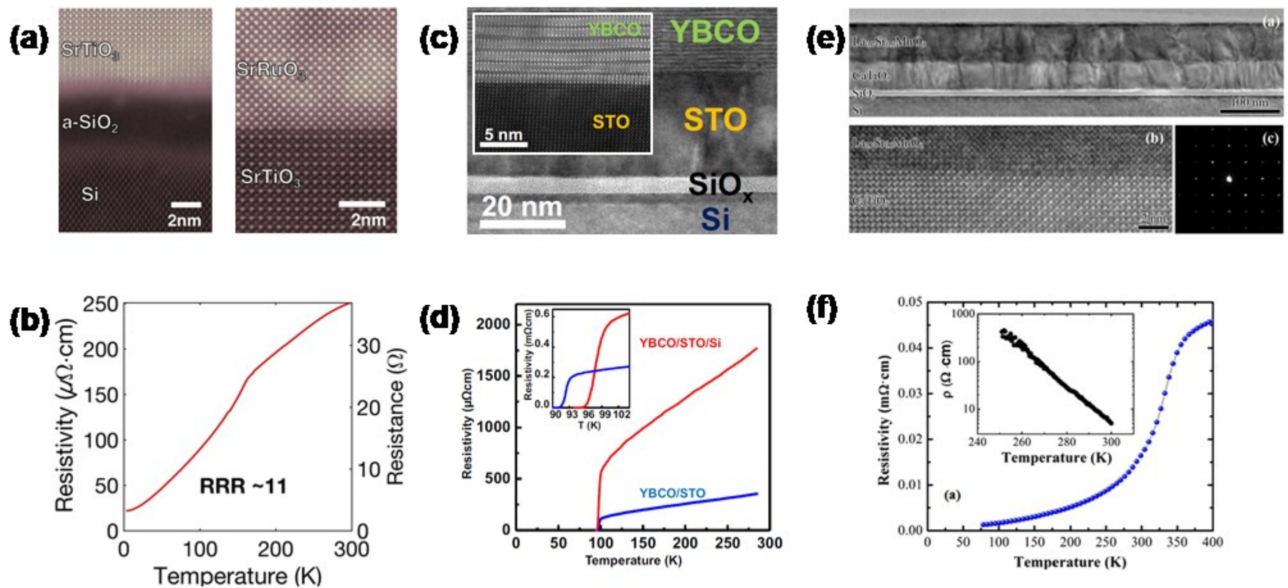

Figure 9. Structural and electronic properties of decoupled oxides on semiconductors. SRO/STO/Si structures showing (a) close-ups on the STO/Si (left) and SRO/STO (right) interfaces, (b) resistivity-temperature curve showing a high residual resistivity ratio indicative of high quality STO films. Reproduced under the terms and conditions of the Creative Commons Attribution license.[146] Copyright 2018, The Authors, published by AIP Publishing LLC YBCO/STO/Si structure showing (c) the entire stack (inset shows a close-up of the YBCO/STO interface) and (d) resistivity-temperature curves showing the critical superconducting temperature in comparison to YBCO grown on STO substrates (insets shows a close-up of the transition region). Reproduced with permission.[147] Copyright 2018, Springer Nature. LSMO/CTO/Si structures showing (e) the entire stack, LSMO/STO interface and electron diffraction and (f) resistivity-temperature curve (the inset showing the behavior of CTO/Si for reference). Note that all these examples feature a typical SiO_x interface layer of at least several nm, which is the consequence of the high oxygen activity required to fully oxidize the functional top layers. Reproduced under the terms and conditions of the Creative Commons Attribution 3.0.[149] Copyright 2015, The Authors, published by AIP Publishing LLC.

3.4.1. $SrRuO_3$

$SrRuO_3$ (SRO) is a conducting oxide that has been extensively used as an electrode material for ferroelectrics.[155] In addition, SRO's ferromagnetism and large magnetocrystalline anisotropy[156] are of interest for the realization of topological magnetic phases.[157,158] The residual resistivity ratio (RRR), defined as ρ_{300K}/ρ_{4K} where ρ is the resistivity, provides a helpful benchmark for assessing the

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quality of a metallic oxide film. A high RRR indicates the film has a low density of defects, such as point defects and, in the case of SRO, orthorhombic domain boundaries.[159]

In a recent work, high-quality SRO films were demonstrated on STO-templated Si.[146] Wang et al. optimized the SRO crystalline quality by implementing a self-limiting growth window.[146] The growth conditions required for obtaining high quality SRO include high temperatures and high oxygen reactivity, which result in a thin amorphous SiOx layer at the STO/Si interface (Figure 9a). The high crystalline quality is evident by a RRR value of ~11 (Figure 9b, which is the highest value reported on Si, and comparable to some of those reported for epitaxial SRO on single crystal oxide substrates.[146]

3.4.2. $La_{1-x}Sr_xMnO_3$

$La_{1-x}Sr_xMnO_3$ (LSMO) is an archetype member of the hole-doped rare-earth manganite family, $R_{1-x}A_xMnO_3$, where R is a trivalent (typically) rare-earth ion and A is a divalent alkaline earth ion. This material system is host to a variety of fundamentally and potentially technologically important phenomena that have drawn interest for many years.[160] Manganites exhibit ferromagnetism mediated through double-exchange, colossal magnetoresistance, and various charge, spin and orbital ordered phases that can co-exist.[161–166] LSMO is commonly used as a conductive electrode for ferroelectrics,[167] similarly to $SrRuO_3$. Moreover, LSMO has been successfully coupled to ferroelectrics to realize magnetoelectric interactions[168,169] Integration of manganites on semiconductors is thus a natural step in exploiting this material in devices.

Méchin et al., successfully integrated LSMO on Si using oxide MBE.[148] A 20 nm thick STO template was first grown, followed by LSMO (x=0.3) films that ranged in thickness from 10-100 nm. The authors reported rocking curve widths <0.33° and rms roughness <1 nm for the 10-100 thick LSMO films. The room temperature resistivity was found to be in the low 1 mΩ·cm range (Figure 9f), which

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is similar to bulk,[170] the Currie temperature was found to be between 320-345K, which is not far below the ~360 K reported for bulk. The authors subsequently reported the use of $CaTiO_3$ (CTO) as a substitute for STO in the buffer layer.[149] The rocking curve for LSMO grown on CTO buffered-Si is over twice as wide (~0.7°) in comparison to the films grown on STO buffered Si.[148] Electron microscopy reveals the formation of amorphous SiO_x layer at the CTO/Si surface (Figure 9e), which is an expected consequence of the high oxygen reactivity necessary to properly oxidize manganese. Altogether, these studies[148,149] present successful integration of LSMO on STO- and CTO-templated Si, with properties that are comparable to those of bulk LSMO. Section 4.2 demonstrates how LSMO integration on Si constitutes a critical building block for device applications.

3.4.3. EuO

EuO is an intriguing ferromagnetic oxide as it has a spin polarization that exceeds 90%,[171] that can be further enhanced with rare-earth doping.[172–175] Given these properties, EuO is an ideal candidate material for spintronics.

In this regard, diamond is particularly attractive for spintronic and quantum applications, owing to the long spin coherence times of its nitrogen-vacancy defects, or N_V centers.[176] Diamond is a wide bandgap semiconductor with unique and attractive properties. Similar to GaN, diamond is attractive for power and RF devices,[177] owing to its large band gap and breakdown strength, high saturation drift velocity and carrier mobility, and high thermal conductivity, which exceeds all other solids (Table 1). Diamond's lattice constant is too small for the epitaxial growth of most perovskite oxides; for example, it is -9.5% mismatched with STO. Fortunately, diamond has a small (~1.9%) mismatch with cubic EuO (lattice constant ~5.14 Å), if the unit-cell of the latter is rotated in-plane by 45° with respect to the unit-cell of the former, i.e. $(001)_{EuO}\|(001)_{Diamond}$,$[110]_{EuO}\|[010]_{Diamond}$ (**Figure 10a**).

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Melville et al., first demonstrated growth of EuO on commercial single crystal diamond substrates[178] (Figure 10), as well as on epitaxial films of chemical vapor-deposited (CVD) diamond. Growth was done using an adsorption controlled technique under low oxygen background pressure, which enabled unoxidized Eu to evaporate from the surface,[179] thereby ensuring a correct Eu:O stoichiometry. The success of this approach is manifested in the magnetic properties of the epitaxial layer. EuO grown on single crystal diamond substrate exhibits a bulk-like (69K) Curie temperature (Figure 10c) and a low temperature saturated magnetization of 5.5 μ_B per Eu ion (Figure 10d). A similar Curie temperature is observed for EuO grown on the epitaxial diamond grown on Si, whereas the saturation magnetization value is 2.1 μ_B per Eu ion. The magnetization in both cases is lower than the prediction of 7 μ_B for Eu^{+2} ($4f^7$).[171]

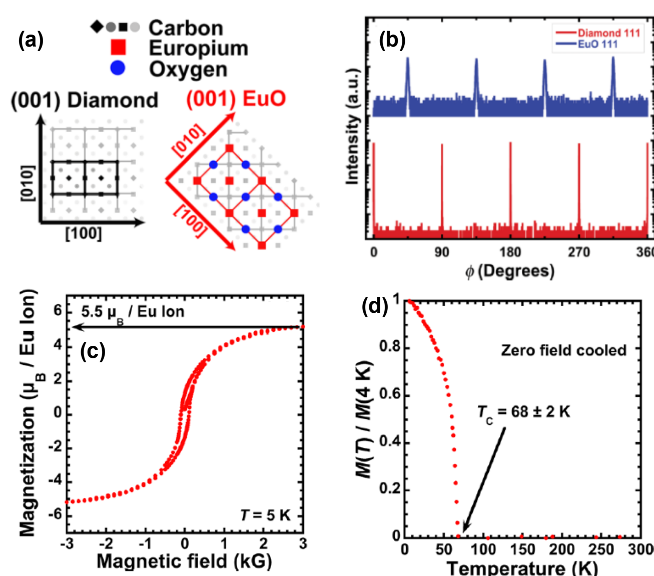

Figure 10. Cubic EuO integration on diamond. The 45° in-plane rotation of (001) EuO on (001) diamond as the epitaxial relation, shown by (a) schematic top view and (b) experimentally verified using ϕ-scans. Magnetic properties of a 37 nm EuO film epitaxially grown on single crystalline diamond substrate with (c) relative magnetization-temperature behavior and (d) low temperature hysterezis loop. Reproduced with permission.[178] Copyright 2013, Amerian Institute of Physics.

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Aside from diamond, Schmehl et al. have studied the growth and properties of EuO on single crystal $YAlO_3$ substrates, (001) Si, and (0001) GaN.[171] Several monolayers of SrO were deposited on the Si surface before EuO deposition in some of the samples. The authors observe similar Curie temperatures for both semiconductors and for films grown on $YAlO_3$. Magnetization values of 6.6 μ_B/Eu has been measured for films on Si and $YAlO_3$. A follow-up work has observed EuO/Si defects which were identified as $EuSi_2$, as well as higher-valence Eu ions.[180] Caspers et al. proposed a surface engineering approach that employs hydrogen passivation and Eu protective layers to minimize such interface defects.[181] EuO/Si epitaxy without SrO buffers has been extensively reported as well,[182] where a conduction band offset of 1 eV has been measured between EuO and Si.[183] Guo et al. have also demonstrated growth of EuO on Si, in which a STO buffer was used to mediate epitaxy.[184] Interestingly, the STO buffer layer also served as a source of oxygen during growth of the EuO film.[185]

It should be noted, EuO is unstable in air where it rapidly oxidizes to the more stable Eu_2O_3 and Eu_3O_4 phases. Consequently, epitaxial EuO must be capped prior to breaking vacuum after growth. Aluminum or amorphous silicon have been used as capping layers; further procedures for capping are discussed in the supplementary information of Schmehl et al.[186]

3.4.4. High Temperature Superconductors

Superconductors integrated on semiconductors are of interest for sensors (e.g. Josephson junctions) and quantum information processing. High-temperature superconducting cuprates could potentially extend some of these applications to higher temperatures, given the higher transition temperatures the exhibit.

Ahmadi-Majlan et al. demonstrated the integration of $YBa_2Cu_3O_{7-\delta}$ (YBCO) on Si using STO-buffered (001) Si.[147] The 30 nm thick STO buffer was grown by MBE, upon which a 50 nm thick

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film of YBCO was grown by PLD. The high temperatures and oxygen pressures used for the PLD growth resulted in SiO_x at the STO-Si interface (Figure 9c). A high critical temperature of 93 K was reported which was even higher than the critical temperature of a YBCO film grown on a single crystal STO substrate under identical conditions (Figure 9d). This enhancement in critical temperature was attributed to a higher concentration of dislocations in the YBCO film on Si, where dislocations may enhance oxygenation.

Beyond Si, Panna et al. have demonstrated the PLD growth of $YBa_2Cu_3O_{7-\delta}$ directly on GaN.[187] The authors took advantage of the high thermal and chemical stability of GaN to grow YBCO directly on GaN using PLD, without an intermediary buffer layer. Good electrical contact between the YBCO and GaN was established. In-plane resistivity measurements exhibit a critical temperature of ~80K, and the authors also analyzed the transport across the interface, observing a super-Schottky diode,[188] which is a diode with a very low turn-on voltage.

3.4.5. Ferroic Nanocomposites

Aside from the creation of layered structures comprised of isostructural perovskites, oxides exhibiting different crystal structures can also be combined in nanocomposites that self-organize into segregated nanoregions. A canonical example of such nanocomposites is the $BiFeO_3$-$CoFe_2O_4$ (BFO-CFO) system, comprised of vertical ferrite CFO nanopillars imbedded in a perovskite BFO matrix.[189,190] Such nanocomposites provide an attractive approach to increase magnetoelectric coupling.[191–193] In this system, the magneto-electric coupling was found to be mediated by strain[194,195] between the piezoelectric BFO matrix and the magnetostrictive CFO particles. In principle, epitaxial strain from the substrate can also play an important role in the magneto-electric coupling of these materials.

Kim et al. have used PLD to grow BFO-CFO nanopillar composites on STO buffered Si.[196] Similar out-of-plane saturation magnetization values (~70 kOe) have been measured on the BFO-CFO

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composites grown on Si as compared to composites grown on single crystal STO substrates. A large magnetic anisotropy was measured on the BFO-CFO nanocomposites grown on STO buffered Si which was not observed for composites grown on STO substrates. This may be the result of strain, as the in-plane lattice constant of STO grown on Si differs from bulk crystals, or imperfect stoichiometry[55] (see discussion in Section 3.5). We also note that BFO-CFO composites have also been grown by sputtering[197] and ALD,[198] which further facilitates possible integration for applications.

3.5. Oxide Heterostructures Featuring 2D Electron Gases

The common perovskite structure of functional oxides provides incredible latitude in creating layered heterostructures comprised of compositionally dissimilar oxides. Such artificial heterostructures contain interfaces where the structural and electronic degrees of freedom of the constituent oxides can be coupled to realize functional behavior.[199]

In particular, interfaces between polar and non-polar oxides have been found to exhibit high density electron gases (2DEG)[200–202]. Such 2DEGs exhibit a variety of phenomena, such as Rashba spin-orbit coupling, superconductivity, and magnetism. Oxide 2DEGs were originally reported at the $LaAlO_3$ (LAO) / STO interface,[200] which has since been studied extensively. Oxide 2DEGs found at interfaces between polar rare-earth titanates and STO have also received considerable investigation. Materials include $NdTiO_3$,[203] $LaTiO_3$,[204] $SmTiO_3$,[205] and $GdTiO_3$ (GTO).[206–208].

The physical origin of the 2DEGs, particularly for the LAO/STO system, has been under considerable debate. One proposed explanation for 2DEGs suggests an *electronic reconstruction* that occurs at the interface, in which charge is transferred from the LAO valence band to the STO conduction

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band.[200,209] This common explanation is based on polar discontinuity at the interface, and is often refered to as the *polar catastrophe*.[210] Competing explanations suggest ionic defects such as oxygen vacancies,[211,212] or cation intermixing[213–215] are the dominant mechanisms behind the emergence of the 2DEGs. The observation of 2DEGs at oxide interfaces between an amorphous polar oxide and crystalline STO seems to preclude the scenario of an electronic reconstruction.[216,217] Yet, a recent report of a 2D hole gas in LAO/STO heterostructures provides compelling evidence for electronic reconstruction, as such a hole gas has long been predicted to be an accompanying effect.[186,218] These competing viewpoints provide a glimpse into the complexity of oxide interfaces and the lively ongoing debate surrounding the physics that governs their behavior.

Regardless of the mechanism(s) that may give rise to oxide 2DEGs, the phenomena they exhibit hold great potential for device applications. Channels for field effect devices are one possible application area, since the electrons of the 2DEGs are confined between two high-k dielectrics. Indeed, in a few short years since their first demonstration,[219] oxide 2DEGs FETs have made considerable progress.[220–222] Recent milestones include integrating 700,000 devices on a 10×10 mm^2 chip[223] that includes inverters and other functional circuits, and miniaturization levels where short-channel effects become appreciable.[224] In addition to FETs, spintronic[225,226] and superconducting[227] devices based on oxide 2DEGs have been demonstrated. Chemical[228,229] and optical[230,231] sensors based on modulating the conductivity of oxide 2DEGs have also been attracting recent attention. Another attractive feature of oxide 2DEGs stems from the ability to 'write' nanoscale conductive regions using a scanning probe tip, enabling so-called *sketched devices* to be created.[232,233] Such sketched devices open routes to study fundamental phenomena,[234,235] or create nano-scale devices for logic[236] and sensing.[237]

Given the functionalities that oxide 2DEGs offer, we consider their integration with conventional semiconductors as a natural advancement towards scalable technology. Oxide 2DEGs offer functionalities that are electrically uncoupled from the semiconductor as well as functionalities that

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arise from electrical coupling to the semiconductor. The former are observed in systems in which the oxide 2DEG is spatially separated from the semiconductor via a thick oxide buffer layer. The latter functionalities emerge as the 2DEG is in intimate contact to the semiconductor, which enables charges from the 2DEG to transfer to the semiconductor (**Table 6** and **Figure 11**).

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Table 6. A chronological summary of the milestones of oxide 2DEGs integration with semiconductors. Structures containing LTO, which is grown at lower oxygen pressure, exhibit an order of magnitude higher carrier densities compared to the rest. These values are also an order higher than the polar catastrophe prediction of ~3×10^{14} cm^{-2}.

Milestone	Semiconductor Interface	Structure	Carrier density (cm^{-2}/interface)
'Remote' Integration STO/Si as a virtual substrate[150]	~10 nm SiO_x	LAO/STO/SiO_x/Si	~10^{14}
'Intimate' Integration on Si[19,152,153,238]	atomically abrupt	LTO/STO/Si GTO/STO/Si	~10^{15} ~10^{14}
'Coupling' 2DEGs carriers in Si[10]	atomically abrupt + band engineering	LTO/STO/Si	10^{13} (in Si) ~5×10^{14} (in oxide)
Intimate Integration on Ge[154]	atomically abrupt	LTO/STO/Ge	>10^{15}
2DEGs integration on GaAs[55]	unknown	GTO/STO/Si	10^{14}

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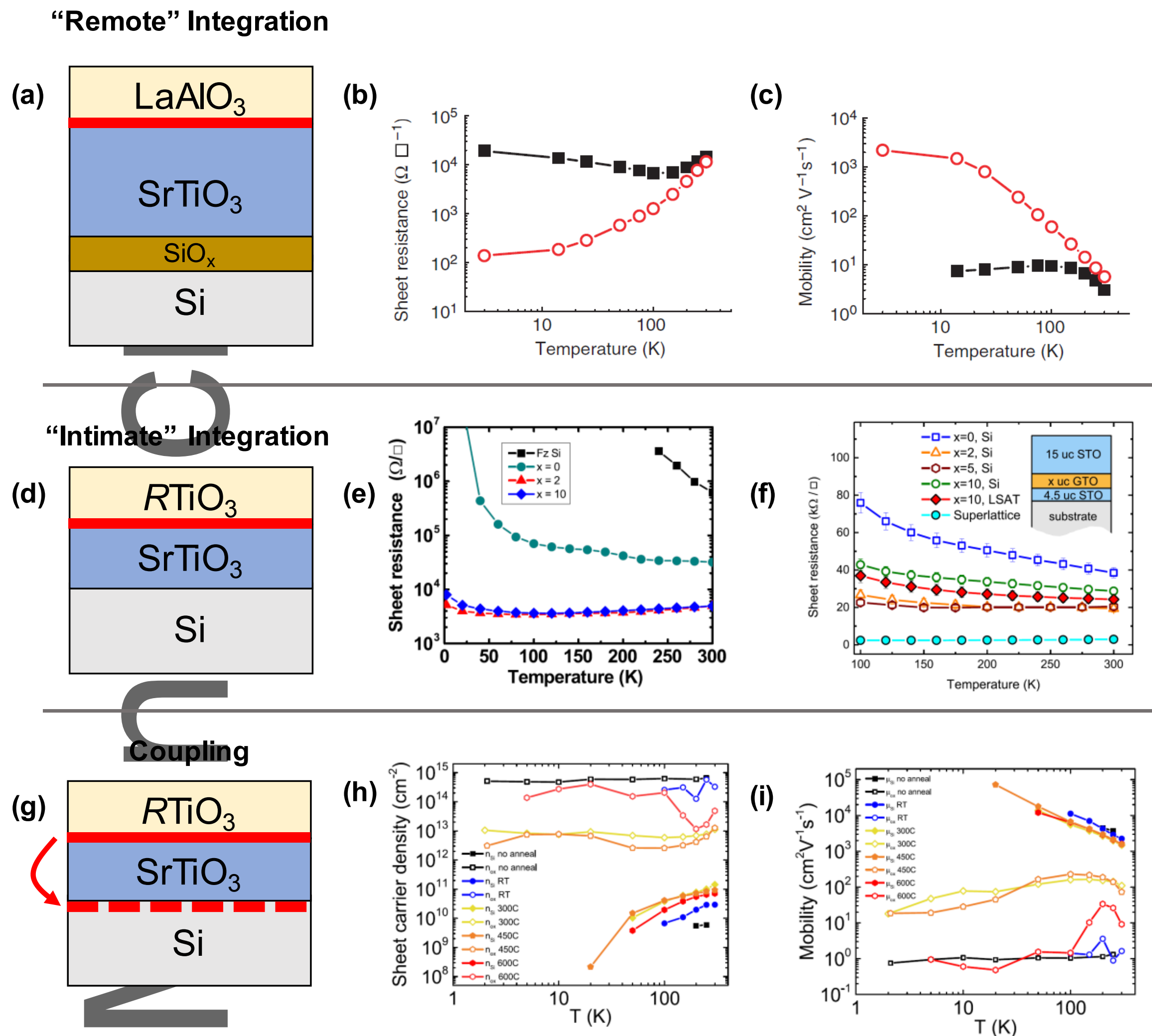

Figure 11. Types and examples of 2DEG integratio with Si. (a) Schematic of LAO/STO remote integration, based on this STO with interfacial SiO_x. Temperature dependence of the (b) Sheet resistance and (c) mobility. The red data points are taken from LAO grown on an STO substrates for comparison. Reproduced with permission.[150] Copyright 2010, Springer Nature. (d) Schematic of intimate integration, where the STO/Si is atomically abrupt and the STO layer is a few unit-cells thick. Temperature dependence of the sheet resistance for various *R*TO thickness for (e) LTO/STO/Si (Reproduced under the terms and conditions of the Creative Commons Attribution 3.0 Unported License.[19] Copyright 2015, The Authors, published by AIP Publishing LLC.) and (f) GTO/STO/Si (Reproduced with permission,[152] Copyright 2015, Amerian Institute of Physics). (g) Schematic of coupling between the 2DEG and the semiconductor, where electrons are pushed from the oxide into the semiconductor. Temperature dependence of (h) the sheet resistance and (i) the mobility of LTO/STO/Si under various oxygen anneals, used for band engineering with the Si.[10] Each color (anneal) shows two plots, one for high density, low mobility electrons (oxide 2DEG) and another for high mobility, lower density (electrons from the 2DEG now in Si), inferred from systematic non-linear Hall analysis. Reproduced under the terms and conditions of the Creative Commons Attribution

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The $LaAlO_3/SrTiO_3$ (LAO/STO) system is the first oxide 2DEG heterostructure to be integrated on a semiconductor.[150] As a first step, a 100 nm layer of MBE-grown STO/Si was aggressively annealed (900°C, 1 atm. O_2), to yield crystalline quality that is comparable to single crystal STO substrates. In essence, the thick STO film on Si becomes a 'virtual substrate'[45,47,48] for the subsequent growth of LAO using PLD.

The transport properties of the LAO/STO/Si heterostructures are comparable to those of LAO/STO samples based on single crystal STO substrates. (Figure 11b,c). In particular, the transition from insulating to conducting behavior at the critical thickness of 4-u.c. of LAO was reproduced. The most significant difference is the low temperature mobility, which is lower by more than two orders of magnitude for the LAO/STO/Si heterostructures in comparison to growth on STO single-crystal substrates. At low temperatures, the mobility of STO is highly sensitive to structural defects.[239] As will be seen and discussed further in the next section, these values are on the higher end of the spectrum of most 2DEGs on semiconductors. Nanoscale sketched devices were created by applying voltages to a scanning probe tip on a LAO/STO/Si structure with a 3-u.c. thick layer of LAO, which is just below the critical thickness for conductivity.[232,233] The demonstration of sketched devices in LAO/STO/Si heterostructures represents key progress in integrating the functionality of oxide 2DEGs on a technologically relevant platform.

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In comparison to the LAO/STO system, RTO/STO systems exhibit a continuous Ti-O sublattice across the polar/non-polar interface, as well as higher electron sheet densities[240] (~10^{14}-10^{15} cm^{-2}). The continuous Ti-O sublattice across the polar/non-polar RTO/STO interface makes this system compositionally simpler than the LAO/STO system. Such RTO/STO heterostructures have been integrated on Si, Ge and GaAs, as discussed below.

Growth on Si

Jin et al. explored the growth of $LaTiO_3$ (LTO) / STO structures on Si (Figure 11e) that had atomically-abrupt interfaces.[19] This was done by sandwiching the Mott insulator LTO between an STO/Si template at the bottom, and an STO protective overlayer, aimed to prevent over-oxidation of the LTO.[241] To avoid LTO over-oxidation during growth, the O_2 background pressure was lowered by ×5 of that used for the growth of the STO layers.[19] Over-oxidation during growth is of particular concern as LTO may transform to the $La_2Ti_2O_7$ pyrochlore phase, which would be detrimental to the structure of the stack. However, a consequence of the low oxygen pressures needed for growth is the creation of oxygen vacancies in the STO which act as n-type dopants. In their first paper, Jin et al. have measured ~9×10^{14} cm^{-2} carriers per LTO/STO interface, which is three times higher than the most ideal and simplified polar catastrophe model.[209,240] It was shown that the sheet carrier density scales with the number of interfaces, thus the vacancies are most likely situated near the LTO/STO interface, rather than in the volume (‘bulk’) of the STO layers.[19]

Kornblum et al. studied the growth of $GdTiO_3$/STO (GTO/STO) heterostructures on Si (Figure 11f), as GTO is less prone to over-oxidation in comparison to LTO. GTO/STO alternating multilayers were successfully integrated on Si using the same oxygen background pressure (5×10^{-7} Torr) for all the layers during growth.[152,153] The GTO/STO structures exhibit atomically abrupt oxide/Si interfaces.[152] X-ray diffraction of the GTO/STO structures grown on Si show comparable structure

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and quality to an identical structure grown under the same conditions on $(LaAlO_3)_{0.3}(Sr_2AlTaO_3)_{0.7}$ (LSAT) single-crystal oxide substrates.[207,242] Indeed, these layered GTO/STO heterostructures produced ~9×10^{13} cm^{-2} electrons per interface, exactly an order of magnitude less than the LTO/STO structures[243] (Table 6).

In a related study, Ahmadi-Majlan et al. created STO/LTO/STO sandwich heterostructures on Si in which metal-insulator behavior could be tuned.[238] The top STO layer was kept very thin (~0.6 nm), and the bottom STO layer in contact with the Si was varied between 2-6 nm. Total carrier densities of ~2×10^{15} cm^{-2} (or ~1×10^{15} cm^{-2}/interface) were measured, consistent with those measured in heterostructures grown by Jin et al.[19] The key finding was a metal-insulator transition that could be tuned with the thickness of the bottom STO layer. The metal-insulator-transition exhibited characteristics that were consistent with a Mott-driven transition, suggesting oxide 2DEGs could provide a pathway to manipulate strongly correlated devices, such as a Mott-transistor,[244,245] directly on Si.

Bringing oxide 2DEGs in close proximity to a semiconductor, while maintaining an atomically-abrupt interface can increase the functionality of these structures. This “intimate” integration scheme (Figure 11d) can potentially enable the exchange of charge and spin between the 2DEG and the semiconductor via electrostatic gating. Semiconductors exhibit higher thermal conductivities, longer spin coherence times, and room temperature mobilities that are 2-3 orders of magnitude higher than oxides (**Table 1**). These properties of semiconductors complement those of oxides, thus making the union, or **Coupling** between the two attractive for future device concepts (Figure 11g).

A major milestone towards this goal was recently achieved by Jin et al., who demonstrated charge transfer from an oxide 2DEG into Si.[10] As discussed in Section 2.2.2, the band alignment between STO and Si can be tuned with oxygen content at the interface.[83,90] The authors systematically

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oxygen-annealed the bottom 1.8 nm-thick STO layer in varying conditions to engineer the interfacial oxygen content. Combining electrostatic simulations and interfacial chemical analysis, the authors have developed a scheme for controlling the band structure without forming an excess of insulating SiO_x at the interface. The Hall signal exhibited highly non-linear behavior, consistent with conduction from multiple channels. Analysis of the Hall behavior using a multi-channel model revealed a sheet carrier density of ~10^{13} cm^{-2} with a room temperature mobility exceeding 100 $cm^2V^{-1}s^{-1}$, consistent with carriers being transferred to the Si[10] (Figure 11h,i). Other conduction channels were ascribed to intrinsic carriers in the undoped Si substrate. By demonstrating electrical coupling between oxide 2DEGs and silicon, this work lays the groundwork for combining correlated oxide physics with high-mobility materials.

Growth on Ge

While Si constitutes the most important and widely used semiconductor, its strong affinity to bind with oxygen remains a challenge for maintaining an abrupt interface with an epitaxial oxide. As discussed in the high-k insulator context (Section 3.1) Ge on the other hand, provides a convenient semiconductor substrate for oxide epitaxy, since its lower tendency to oxidize allows a wider oxide growth window. Germanium's larger lattice constant (Table 1) needs to be considered with respect to STO, but this has been successfully addressed,[12,86,92,246] as discussed in Section 2.1.1.

Edmonson et al. have recently published a thorough investigation of LTO/STO 2DEGs grown both on STO substrates and on STO buffered Ge.[154] This work showed clear evidence of oxygen scavenging from the STO substrate during LTO growth (as previously shown for growth of EuO on STO[184] or deposition of some metals over STO[247]). Since STO substrates are a richer source for oxygen compared to a thin (~3.2 nm) STO/Ge template, the best LTO films can be grown on STO substrates at 10^{-10} Torr, versus 10^{-7} Torr of oxygen background necessary for growth on thin STO buffered Ge.

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High-resolution energy loss near-edge spectroscopy (ELNES) mapping revealed significant reduction at the LTO/STO interface, confirming the presence of oxygen vacancies, consistent with the prior studies of Jin et al.[19] A thorough investigation has yielded the optimized structure of 12 nm LTO / 3.2 nm STO / Ge (**Figure 12a**), which exhibits sheet densities of ~2.5×10^{15} cm^{-2} and mobilities of ~6 $cm^2V^{-1}s^{-1}$ (Figure 12b-d). This mobility is higher than that obtained for 2DEGs on GaAs and Si, suggesting higher crystalline quality for STO grown on Ge. Tensile strain imparted by the Ge to STO may play a role in the mobility enhancement as well.

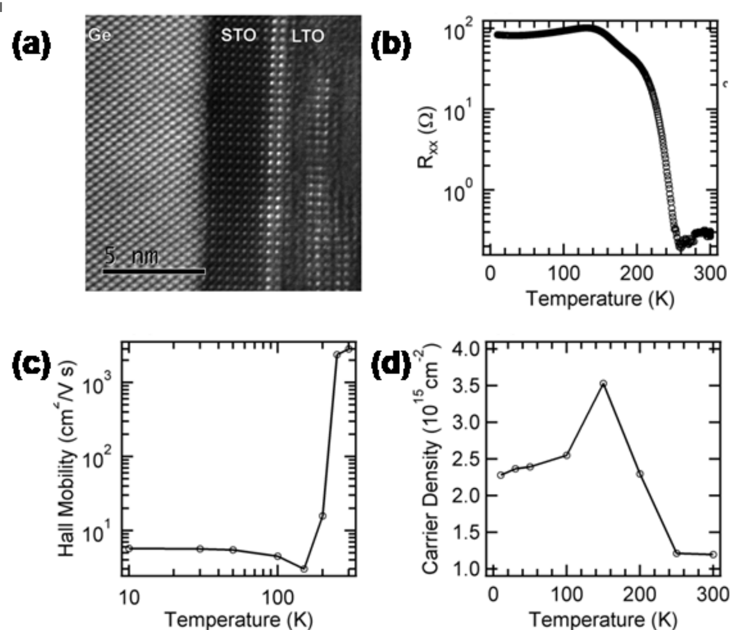

Figure 12. Structural and electronic properties of LTO/STO 2DEG on Germanium. (a) Cross sectional TEM micrograph. (b) Sheet resistance, (c) Hall mobility and (d) sheet carrier density versus temperature, all showing the effect of freeze-out of the carriers of the donor-doped Ge, occurring at a 100-200 K range. Reproduced with permission.[154] Copyright 2018, Amerian Institute of Physics.

Growth on GaAs

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Group III-V semiconductors are an attractive candidate for the integration of oxide 2DEGs to extend the potential for device functionality, particularly in regards to optoelectronic applications. The GTO/STO on Si structures described above have also been grown on GaAs by Kornblum et al.[55] A homoepitaxial layer of GaAs was grown on a GaAs wafer and then capped with a layer of arsenic to enable *ex-situ* transfer to an oxide MBE system for the growth of the GTO/STO layers (see Section 2.1.5). The growth of GTO on STO-buffered GaAs required a short 665°C anneal in vacuum to obtain crystallinity. In terms of electrical transport, Hall measurements indicate electron sheet densities of ~2×10^{14} cm^{-2} electrons per interface (**Figure 13**), which is higher than sheet densities of GTO/STO grown on Si or oxide substrates. Oxygen vacancies likely also play a role in slightly increasing the sheet carrier densities of the structures on GaAs. In addition, the lower mobility values observed in this work[55] further indicate imperfections of the crystalline structure. This is particularly emphasized at low temperatures, where the best quality epitaxial STO films[239,248] demonstrate values larger by more than $\times10^4$. This observation outlines the important limitations of such oxide integration schemes: the extremely narrow growth window that is mandated by the need to preserve the semiconductor limits the crystalline quality, at least using current growth schemes.

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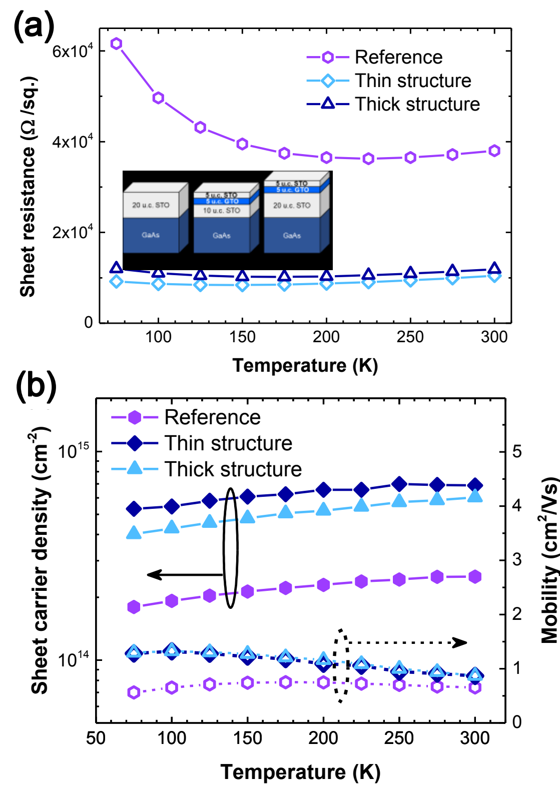

Figure 13. Transport properties of GTO/STO oxide 2DEGs structures integrated with GaAs.[55] (a) Sheet resistance as a function of temperature. Inset is a schematic structure of the three stacks, where the reference sample is STO/GaAs grown under the same conditions, whose conductivity is attributed to oxygen vacancies alone. (b) Mobility and sheet electron density as a function of temperature. Reproduced with permission.[55] Copyright 2018, Amerian Institute of Physics.

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4. Emerging Applications

In the following section our discussion progresses towards emerging device applications that leverage the functionality of semiconductor-oxide heterostructures. The applications discussed here, which include micro-electromechanical systems (MEMS) actuators and sensors, optical modulators for silicon photonics and heterojunctions for photocatalysis, highlight the broad impact epitaxial oxides on semiconductors can potentially have on technology development.

4.1. MEMs actuators

In general, the electronic properties of multifunctional oxides are strongly coupled to the crystal lattice. This coupling between electronic and structural degrees of freedom allows electronic behavior to be controlled by introducing changes to the physical structure. Tuning of electronic properties of oxides through structural changes has been studied extensively in epitaxial films, in which compressive or tensile strain can be imposed via the substrate,[49,249] and also in bulk single crystals.[250,251] Examples include the enhancement of ferroelectricity in $BaTiO_3$,[252] control of ferromagnetism in $SrCoO_{3-\delta}$,[253,254] and the tuning of superconductivity in Sr_2RuO_4.[255]

In terms of applications, this interplay between electronic and structural degrees of freedom could lead to novel functionalities that can be exploited in microelectromechanical systems (MEMS). Silicon remains the predominant platform for the development of MEMS devices. Thus, the growth of single crystalline multifunctional oxides on silicon opens a practical pathway for the integration of these materials in MEMS.

In particular, piezoelectric materials can be exploited for transduction and actuation, which are two key functionalities of MEMS. The ability to epitaxially grow oxides on Si has enabled single crystalline piezoelectric films to be utilized, whereas polycrystalline piezoelectric materials have been

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predominantly utilized to date.[256] Baek et al. utilized a single crystalline $SrTiO_3$ (STO) base layer in conjunction with a miscut substrate to integrate single crystalline $Pb(Mg_{1/3}Nb_{2/3})O_3$-$PbTiO_3$ (PMN-PT) films on Si[257] (**Figure 14a,b**). The combination of STO and the miscut substrate enables the normally volatile PbO to be incorporated into the films, while avoiding the formation of secondary phases. The PMN-PT bimorph cantilevers exhibited exceptionally large deflection under modest applied fields. Besides the piezoelectric effect, the flexoelectric effect can also be utilized for actuation in MEMS. The flexoelectric effect induces a polarization in an insulating material through a gradient in strain. Though small in bulk materials, the flexoelectric effect can be pronounced in thin films in which gradients in strain can be engineered.[258] Actuation can be achieved through the inverse effect, namely, the creation of a gradient in strain through an applied electric field. The use of the flexoelectric effect also introduces a simplification to the cantilever device, as the additional passive layer needed in a piezoelectric bimorph structure is unnecessary. Bhaskar et al. exploited the flexoelectric effect to achieve actuation in STO cantilevers integrated on Si[259] (Figure 14c,d). The field-induced curvature exhibited by the STO cantilevers compared well to the curvature of cantilevers comprised of other benchmark piezoelectric materials.

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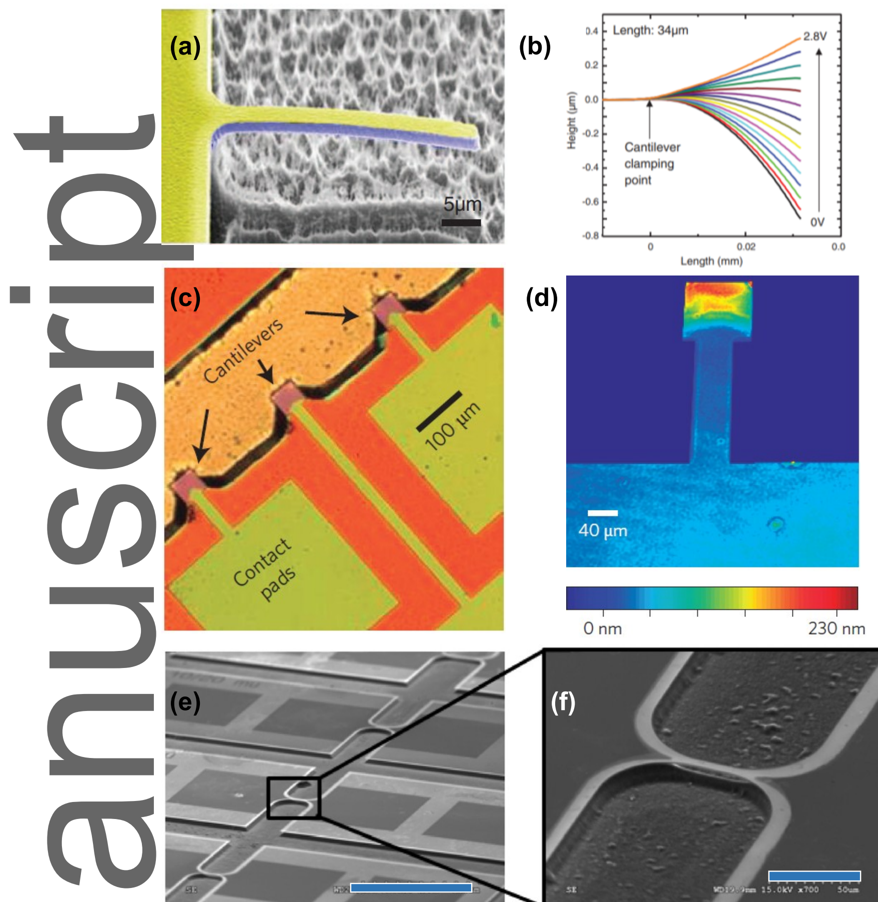

Figure 14. Examples of MEMS devices based on oxide/semiconductor structures. (a) False-color SEM image of a piezoelectric micro cantilever and (b) its displacement profile as a function of DC current. Reproduced with permission.[257] Copyright 2011, The American Association for the Advancement of Science. (c) Optical image of an array of STO cantilevers and (d) a 3D image of one cantilever, where the colors denote the out-of-plane displacement. Reproduced with permission.[259] Copyright 2016, Springer Nature. (e) and (f) SEM images of a LSMO freestanding microbridge used for pressure sensing at low pressures (scale bars are 300 and 50 µm, respectively). Reproduced with permission.[260] Copyright 2015, Amerian Institute of Physics.

4.2. MEMs sensors

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Beyond actuation, the electrical transport characteristics of multifunctional oxides exhibit strong sensitivities to temperature and strain.[49,161,170,249,250] Such sensitivities could be exploited in MEMS devices for uncooled bolometry or pressure sensing. $La_{1-x}Sr_xMnO_3$ (LSMO) is an archetype oxide compound[161,170] that is of interest for such applications. At a composition near x ~ 0.33, LSMO exhibits an insulator to metal transition with decreasing temperature, which is associated with a paramagnetic to ferromagnetic transition.[261,262] Liu et al. realized suspended microbridges comprised of LSMO (x=0.3) on a silicon substrate using standard MEMS processing techniques.[263,264] For uncooled bolometers, thermally decoupling the heat sensitive material from the bulk substrate is critical. The authors demonstrated a reduction in thermal conduction by 4 orders of magnitude. Furthermore, the transport characteristics of the suspended bridges were not degraded after being subject to processing using standard MEMS techniques. These developments bode well for the use of oxides in bolometers and the general integration of oxide materials in MEMS. For pressure sensing, Le Bourdais et al. realized LSMO microbridges on silicon and demonstrated the Pirani effect, in which the temperature dependent resistance of a microbridge is modulated by the cooling effect that gas molecules surrounding it produces[260] (Figure 14e,f). The LSMO microbridges exhibited sensitivities that were more than double those of similar Pirani gauges based on conventional metals. Yet more encouraging, device yields were 95%, which attests to the potential for practical utilization of multifunctional oxides in MEMS sensors. Finally, Pellegrino et al. realized micro cantilever structures based on LSMO for use as piezoresistors, in which mechanical strain alters the electrical conductivity of the material.[265] Although the authors realized their cantilever structures on an STO substrate, integration on Si is in principle achievable based on the microbridges that have been fabricated for bolometry and pressure sensing in the previous examples.

4.3. Electro-optics: Silicon Photonics

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Silicon photonics is another area in which crystalline oxides on silicon could have significant impact. Copper-based interconnects used for intra-/inter-chip communication have become increasingly complex as complementary metal oxide semiconductor (CMOS) technology continues to evolve. The loss, dispersion, crosstalk and ultimate limitations in speed of copper interconnects require the development of a replacement technology. Optical interconnects based on silicon photonics are poised to elevate interconnects beyond the paradigm of charge transport.

For Si photonics, the development of high-speed optical modulators is needed for high bandwidth data transmission. In this regard, ferroelectric $BaTiO_3$ (BTO) integrated on silicon is an ideal candidate material for the development of modulators and other lightwave circuit elements. Associated with its non-centrosymmetric crystal structure, ferroelectric BTO exhibits the Pockels or linear electro-optic effect, in which the refractive index changes linearly with respect to electric field. The electro-optic coefficient of BTO can exceed > 1000 pm/V, which is far larger than the electro-optic coefficient of $LiNbO_3$ (~ 30 pm/V) used in commercially available discrete modulators. Abel et al. first demonstrated the Pockels effect in 130 nm thick BTO films epitaxially grown on Si.[266] For devices, relatively thick films are needed to confine optical modes. Thick BTO films are relaxed with respect to the Si substrate and exhibit an in-plane polarization due to tensile strain that arises from the difference in thermal expansion coefficients between the film and substrate. The authors measured a Pockels coefficient of 148 pm/V for an optical electric field parallel to the c-axis, i.e. beam applied perpendicular to the plane of the film.

The in-plane polarization is suitable for devices in which electric fields are applied laterally across the film via planar electrodes. Using BTO grown on silicon-on-insulator (SOI) wafers, Xiong et al. created various lightwave circuit elements, including Mach-Zehnder interferometers, ring oscillators as well as grating couplers.[267,268] An effective Pockels coefficient of 213 pm/V was determined by evaluating the performance of a Mach-Zehner interferometer for the BTO on SOI films. Electro-optic modulation up to 4.9 GHz was also demonstrated, which frequency was limited only by the device

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drive circuit. Abel et al. have studied the effects of microstructure on the Pockels coefficient, and compared various growth methods, observing a span of two orders of magnitude in this parameter, peaking at 140 pm/V in an early work.[269] In a separate work members of this team have pinpointed a key loss mechanism to the few naometer thick underlying STO layer used for BTO integration with Si.[270] The authors have shown that residual hydrogen in this layer has a dramatic effect on the optical losses, and have developed a low-temperature anneal that removes the hydrogen, showing about a factor of ×25 reduction of the losses to 6 dB/cm for 220 nm Si over 50 nm of BTO.

Most recently, Abel et al. have been able to further improve the material characteristics and device performance of BTO on Si based devices.[271,272] The authors utilized a wafer-bonding technique to create a stacked heterostructure in which BTO is separated from the substrate by a thick insulating layer. The thick insulating layer prevents optical leakage into the substrate thereby isolating the Pockels effect from any potential plasma related modulation effects associated with residual carriers in the Si. The BTO is grown on STO/Si (SOI) wafers, bonded to the target wafer and the original substrate is removed mechanically and chemically. Very large coefficients of r33 = 342 pm/V and r42 = 923 pm/V were measured that enabled optical modulators to exhibit 40 Gbits/s transfer rates (**Figure 15a,b**)). In the same report, Abel et al. also studied plasmonic modulators based on BTO on Si. Such devices allowed for even higher data transfer rates of 50 Gbits/s (Figure 15c,d). These developments bode well for the realization of practical modulators based on BTO on Si. Days before the submission of this review, Abel's IBM group has scaled-up this work and demonstrated monolithic integration of the wafer-bonded BTO onto 200 mm Si wafers.[273]

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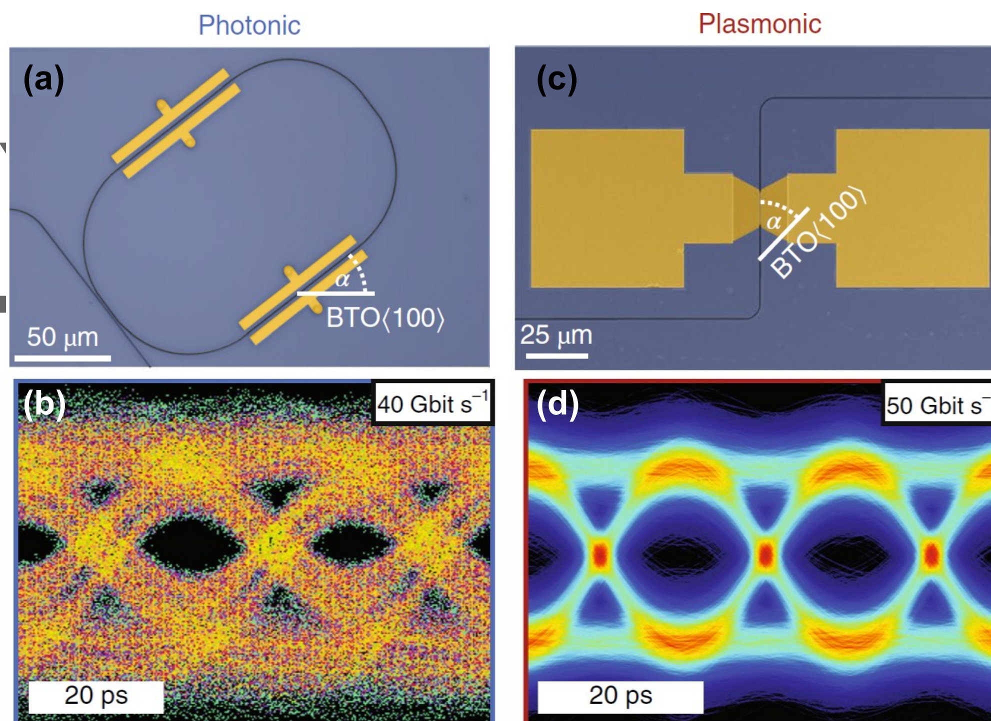

Figure 15. Layout and data transmission eye diagram in (a),(b) photonic and (c),(d) plasmonic devices. Reproduced with permission.[271] Copyright 2018, Springer Nature.

Finally, we note that the electro-optic effect in BTO could potentially be further enhanced through engineering tensile or compressive strain. Density functional theory calculations by Fredricksen et al. found that strain promotes phonon softening, which lead to divergences in the susceptibility that in turn could increase Pockels coefficients.[274] The ability to further enhance the Pockels effect beyond their already large values would be remarkable.

4.4. Photoelectrocatalysis

Photoelectrocatalysis is a striking example in which the complementary properties of oxides and semiconductors can be coupled to address a technological challenge. Developing clean, sustainable

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yet economic sources of energy remains one of the greatest challenges we face. The production of fuel through photoelectrochemical (PEC) means is a promising route to address this challenge. In this regard, water splitting, consisting of the hydrogen evolution reaction (HER) and the oxygen evolution reaction (OER), is the most notable application of PEC reactions,[275–279] as a sustainable source for hydrogen – the cleanest and most energy-dense chemical fuel. Other possible applications include dinitrogen photoreduction to ammonia, carbon dioxide photoreduction to organic compounds, and photo-oxidation of organic species in aqueous environments and others.[280–283]

Conventional semiconductors offer relatively small band-gaps that are ideal for the generation of electron-hole pairs from sunlight (particularly for direct bandgap semiconductors, Table 1), their separation and transport. Unfortunately, their tendency to photo-corrode under photocatalytic conditions renders their practical implementation untenable.[284] In comparison, oxides such as TiO_2, which have been extensively studied, are stable under photocatalytic conditions;yet their large indirect bandgaps severely limit their effectiveness in PEC scenarios. In this regard, hybrid heterojunctions comprised of semiconductors and crystalline-oxides can potentially combine the ideal characteristics of both materials, namely, efficient generation of electron-hole pairs and chemical stability under photocatalytic environments.

Implementation of such concepts does not mandate epitaxial oxides. Hu et al. have demonstrated OER using atomic layer deposition (ALD) of TiO_2 passivation on Si, GaAs and GaP.[278] Owing to the simplicity and scalability of ALD, this approach is very promising. The oxide was coated with thin Ni catalysts, and the authors have used 1.0 M KOH in water (pH 13.7) to demonstrate currents exceeding 30 mA/cm^2 for Si, 14.3 and 3.4 mA/cm^2 for GaAs and GaP, respectively. As expected, some ~10 nm of uncontrolled layer has been observed by the authors at the TiO_2/Si interface. In a follow up work, Verlage et al. have applied the same techniques on a tandem solar cell consisting of Ni/TiO_2/InGaP/GaAs structure, reporting remarkable *unassisted* water splitting with excellent efficiencies.[279] Despite these excellent performances demonstrated by these works, one might expect

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that a more controlled and ordered interface, such as that afforded by epitaxial oxides, would increase performance.

Ji et al., were the first to demonstrate this possibility in a stacked heterostructure comprised of a p-type Si base, an epitaxial $SrTiO_3$ (STO) layer (**Figure 16a**), followed by a nanostructured Pt/Ti bilayer.[285] The latter was nanopatterned using nanosphere lithography into a mesh-like array on the STO surface and played the role of metal catalysts. Given the near proximity between the conduction bands of Si and STO[9] (Figure 16b), photo-generated electrons from the Si base were transported through the STO layer for reaction at the surface. Using a 0.5 M H_2SO_4 (pH 0.3) aqueous solution, operated under a broad-spectrum illumination of 100 mW cm^{-2}, a large photocurrent density of 35 mA cm^{-2} was achieved, accompanied by an open circuit potential of 450 mV. The placement and patterning of photocatalysis on the STO surface added a degree of tunability to the performance of the heterostructure. The heterojunctions suffered no decrease in performance over at least 35 hours of continuous operation.

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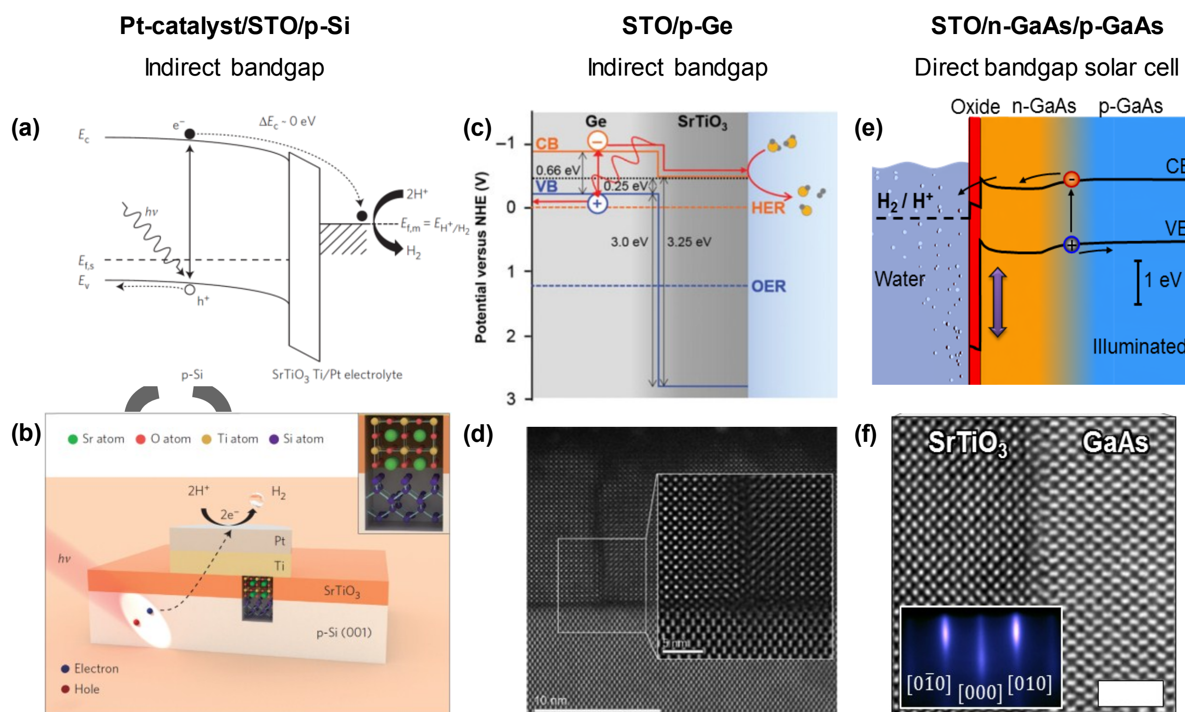

Figure 16. Structure and energetics of epitaxial oxides in photoelectrocatalysis. STO/Si based PEC: (a) band structure and (b) schematic structure. Reproduced with permission.[285] Copyright 2014, Springer Nature. STO/Ge based PEC,[80] (c) band structure at flatband, (d) high resolution TEM image (scale bar is 10 nm), inset showing a close-up on an antiphase boundary (scale bar is 5 nm). Reproduced with permission.[80] Copyright 2018, Cambridge University Press. STO/np-GaAs based PEC, (e) band structure under illumination, (f) high resolution TEM image of the interface (scale bar is 2 nm), inset showing a post-growth RHEED pattern. Reproduced under the terms and conditions of the Creative Commons Attribution 3.0 Unported Licence.[13] Copyright 2017, The Authors, published by the Royal Society of Chemistry.

Following this study, Kornblum et al., explored the use of a direct band-gap GaAs pn-junction solar cell in place of Si.[13] In principle, the direct band-gap of GaAs, and the use of a pn-junction enables more efficient absorption and generation of electron-hole pairs. Their heterojunctions were comprised

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of a 16 nm thick layer of epitaxial STO grown on a GaAs pn-junction (Figure 16f), in which the n-type side of the GaAs interfaced with the STO. With the conduction band of the GaAs situated above the conduction band of the STO,[13] the heterojunction acts as a photocathode: photo-generated electrons from the GaAs can be transported to the STO surface for reaction (Figure 16e). Faradaic efficiencies of 100% for hydrogen evolution were demonstrated, as well as incident photon-to-current efficiencies that exceeded 50%. These results point to the promising application of semiconductor-crystalline oxide heterojunctions for use in PEC reactions. In terms of optimizing semiconductor-crystalline oxide heterojunctions for PEC, work can still be done. For example, Kornblum et al. found that a loss in energy was incurred by the photogenerated electrons transported from n-GaAs to STO, due to the difference in alignment between the conduction bands of the two materials, resulting in a reversed Schottky diode in series that consumes much of the photovoltage. The techniques of band-gap engineering discussed in the preceding sections could be utilized to mitigate these challenges.[10] Despite these low conversion efficiencies, this work featured additional advantages; this half cell operated in an environmentally benign phosphate-buffered solution (PBS) at a pH of 7, whereas other works use strong acids and bases. In addition, this work showed ~100 % Faradaic efficiencies using merely the STO surface and no additional catalysts, whereas other works applied nanostructure Pt-based catalysts, or earth-abundant Ni based catalysts. Altogether, this work has shown promising potential of epitaxial oxides on direct bandgap solar cells for photoelectrocatalysis, and pointed out routes to pushing performance further.

Stoerzinger et al. have leveraged their prior experience with STO/Ge[12,246] to perform HER under neutral pH using PBS solutions at pH 7,[80] implementing a similar approach as above (Figure 16c). One possible advantage of Ge is its low band gap (Table 1) which enables to collect more of the solar spectrum; the tradeoff, however, is low photovoltages. This work found that 13 nm STO block electron transport, but 4 nm STO layer can facilitate PEC. However, the authors found stability issues

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with the films, and attributed them to pinhole and antiphase boundary (Figure 16d) formation in the thin films which degraded the ability of STO to protect the underlying Ge.

4.5. Spin Injection

Integrating ferromagnetic oxides on semiconductors, e.g. via template layers, is a promising direction for spintronic devices. The ferromagnet can filter the spin during injection into the semiconductor,[286,287] resulting in spin-polarized electrons where longer spin coherence times are possible in comparison to oxides. While this concept has been shown with oxide-oxide systems, most commonly with LSMO/Nb:STO,[288] its implementation on semiconductors remains elusive. While template layers such as STO can stabilize semiconductor surfaces, most ferromagnetic oxides require significantly higher growth temperatures and oxygen activities than what semiconductors can withstand. Under the necessary conditions required to obtain a functional ferroelectric oxide, the semiconductor surface will thus be oxidized, forming a barrier for charge transport. This has been shown with electron microscopy to occur even in the highest quality ferrmomagnetic oxides grown on silicon[146,149] (see Section 3.4 and Figure 9). Additional functionality can be gained by adding ferroelectrics and multiferroics to the equation.[169]

These concepts, demonstrated on all-oxide systems, could be highly attractive for integration on semiconductors, if the abovementioned material challenges could be mitigated.

5. Conclusions and Outlook

This article reviewed the current state of epitaxial oxides on semiconductors, progressing from growth to device applications. We conclude by discussing remaining challenges that, if overcome, could

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further expand the functionality of epitaxial oxides on semiconductors and the development of transformative device technologies.

We highlighted the opportunities and challenges of engineering the epitaxial interface. As discussed, band alignment is intimately related to interfacial composition and structure; thus, the ability to control interfacial composition, in particular the oxygen content, will considerably broaden design-space for engineering functional behavior.[10] Besides engineering band alignment, achieving fully oxygenated oxides on semiconductors while maintaining atomically abrupt interfaces is a challenge that needs to be addressed. On the one hand, low oxygen pressure during deposition enables atomically abrupt interfaces that are free of native oxide species to be realized. On the other hand, the low oxygen pressure can create residual oxygen vacancies in the oxide that are generally unwanted. Further studies, e.g. by spatially-tracking ^{18}O isotopes using mass spectrometry could be helpful in this regard.[289] Innovative concepts for minimizing unwanted interface layers that were implemented by the high-k dielectrics community may be useful for epitaxial oxides as well.[290]

Increasing the scalability and throughput of epitaxial growth on semiconductors should be an important objective to extend pathways to practical integration. Efforts to grow epitaxial oxides on semiconductors via ALD[27] and hybrid MBE[46] have shown great promise. Continued effort should be focused on improving the quality of epitaxial films and interfaces grown using these techniques. Another milestone would be the growth of epitaxial oxides directly on Si using ALD without the need of UHV preparation (e.g. native SiO_x removal and template deposition). In parallel with such efforts should be the exploration of simplified growth schemes and the testing of significantly enhanced deposition rates using MBE, as approaches to maximize throughput have yet to be rigorously investigated.

The microstructure of epitaxial oxides deposited on semiconductors, namely, the formation of defects such as dislocations, also presents challenges for the development of highly scaled devices. Since oxides and semiconductors typically belong to different crystal types (e.g. perovskite vs. diamond

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cubic), dislocations nucleate at steps on the substrate surface where the oxide lattice-parameter in the growth direction is incommensurate with the step height. While the presence of dislocations may not adversely affect device performance for some applications, their presence poses challenges to applications in which highly scaled devices are to be created. Developing techniques to minimize the miscut of substrates is needed to minimize steps. Alternatively, engineering the surface of semiconducting substrates to control the location and nucleation points of dislocations would also help.

While alkaline-earth based oxides, such as $SrTiO_3$, have served exceptionally well as intermediary buffer layers between a variety of functional oxides and semiconductors, we challenge the community to develop approaches to grow other oxide materials directly on semiconductors. For example, rare-earth oxides, such as $LaTiO_3$, grown directly on semiconductors could enable new mechanisms for charge transfer given its polar nature. Such polar oxides have received considerable attention in all-oxide heterostructures. The significant challenge of introducing new oxides directly on semiconductors would greatly benefit from theoretical guidance. In this regard, recent leaps in machine learning, in conjunction with first principles calculations,[291] could prove useful in identifying candidate oxides for direct integration, and interfacial structures needed to achieve stable epitaxy.

Realizing robust p-type doping and conductivity in oxides would have broad technological impact in a variety of areas, including epitaxial oxides on semiconductors. In particular, robust p-type doping and conductivity would significantly expand the ability to engineer charge transfer and built-in electric fields across interfaces between semiconductors and epitaxial oxides. P-type doping could further expand the palette of hybrid semiconductor-oxide pn-junctions, p-p heterojunctions etc., that can be realized, when combined with band gap engineering and n-type charge transfer, which have already been demonstrated.

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We reviewed the wide spectrum of material functionalities that can be integrated on semiconductors, ranging from high-temperature superconductors to 2D electron gases, ferromagnets, ferroelectrics, multiferroics and colossal magnetoresistance oxides. We note that for the most part, these advancements constitute the first and critical step of creating building blocks for devices, but actual practical applications are still scarce. We foresee that the continuous advancement of oxide epitaxy – both fundamentally and technically, together with creative ideas, would allow these building blocks to be put together into interesting, useful new devices in the near future. We hope that this overview stimulates ideas for new concepts of functional devices, and lays the groundwork for their implementation.

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TOC Summary

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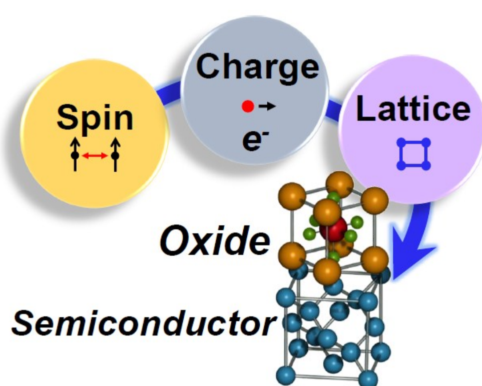
Multifunctional oxides epitaxially integrated on semiconductors provide a platform by which novel device technologies can be realized. The complementary properties between oxides and semiconductors enable functionalities that cannot be achieved in either material alone. This article reviews the epitaxial growth oxides on semiconductors, the material behaviors that integrated heterostructures offer, and emerging device applications.



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