Harnessing Conductive Oxide Interfaces for Resistive Random-Access Memories

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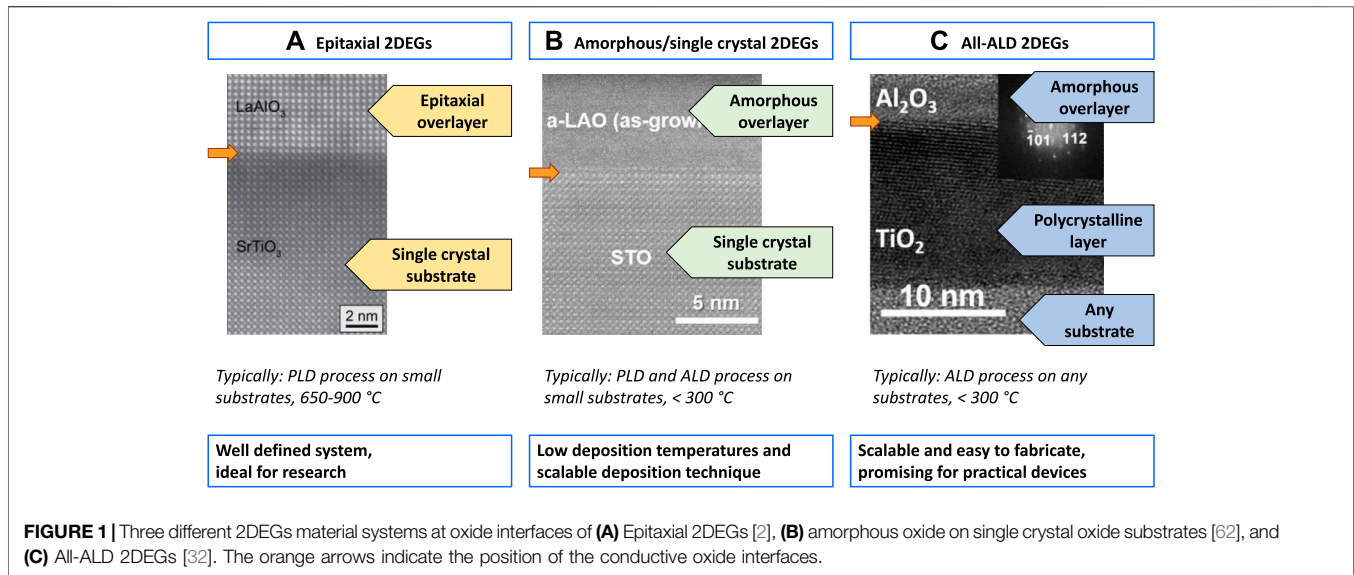
Two-dimensional electron gases (2DEGs) can be formed at some oxide interfaces, providing a fertile ground for creating extraordinary physical properties. These properties can be exploited in various novel electronic devices such as transistors, gas sensors, and spintronic devices. Recently several works have demonstrated the application of 2DEGs for resistive random-access memories (RRAMs). We briefly review the basics of oxide 2DEGs, emphasizing scalability and maturity and describing a recent trend of progression from epitaxial oxide interfaces (such as LaAlO$_3$/SrTiO$_3$) to simple and highly scalable amorphous-polycrystalline systems (e.g., Al$_2$O$_3$/TiO$_2$). We critically describe and compare recent RRAM devices based on these systems and highlight the possible advantages and potential of 2DEGs systems for RRAM applications. We consider the immediate challenges to revolve around scaling from one device to large arrays, where further progress with series resistance reduction and fabrication techniques needs to be made. We conclude by laying out some of the opportunities presented by 2DEGs based RRAM, including increased tunability and design flexibility, which could, in turn, provide advantages for multi-level capabilities.

Keywords: oxide interfaces, resistive random-access memories, device physics, oxide electronics, oxide electronic devices

INTRODUCTION

Two-dimensional electron gases (2DEGs) can be formed at some oxides interfaces [1]. These oxide interfaces provided a fertile ground for the discovery and manipulation of extraordinary physics, such as superconductivity [2–5], magnetism [6, 7], magnetoelectric coupling [8, 9], Rashba spin-orbit coupling [10], persistent photoconductivity [11, 12], and integer/fractional quantum Hall effect [13, 14]. Over the last decade, leveraging these phenomena towards various devices, such as transistors [15–19], diodes [20], gas sensors [21], spintronic devices [22, 23], and memory devices [24–29], has drawn considerable attention. In addition to the exotic phenomena listed above, the emergence of a high sheet density of electrons (typically 10^{12}~10^{15} cm^{-2}) between two insulators is already attractive for some devices, such as in the role of channels or back electrodes. We note that for the sake of convenience and simplicity, we very broadly use the term 2DEGs as a general name for conductive oxide interfaces, covering 2D, quasi-2D systems, and conducting interfaces where the dimensionality is not well-defined.

Oxide 2DEGs were first reported in epitaxial oxide interfaces, where a complex oxide such as LaAlO$_3$ is grown, typically by pulsed laser deposition (PLD), on a single-crystal oxide substrate, typically SrTiO$_3$ [1, 2] (**Figure 1A**). Therefore, forming such 2DEGs requires epitaxial oxide thin film deposition at high temperatures. Exploiting 2DEGs for novel electronic devices will significantly

FIGURE 1 | Three different 2DEGs material systems at oxide interfaces of **(A)** Epitaxial 2DEGs [2], **(B)** amorphous oxide on single crystal oxide substrates [62], and **(C)** All-ALD 2DEGs [32]. The orange arrows indicate the position of the conductive oxide interfaces.

benefit from simplifying the materials and deposition methods, where low-temperature, scalable, and microelectronics-compatible approaches are of considerable advantage. Later work has demonstrated that 2DEGs can be formed at more simple interfaces, between amorphous and single-crystalline oxides [30, 31] with the benefit of room temperature preparation. Recently 2DEGs were shown to form even at amorphous/polycrystalline oxide interfaces [17, 21, 32, 33] (**Figure 1C**). Furthermore, the oxide deposition temperatures were reduced from 650-900°C to 25–300°C, and the deposition techniques have been extended from PLD to the more scalable atomic layer deposition (ALD), which is widely used by the microelectronics industry.

Among their various device prospects, recently, 2DEGs were utilized for resistive random-access memories (RRAMs) [24–28]. RRAM devices [34–36] are highly attractive for the next-generation memories [37, 38] and new computing paradigms [39–46]. The potential of 2DEGs in this role has yet to be critically discussed. In this mini review, we briefly review the oxide material systems hosting 2DEGs, focus on their application in the RRAM devices, and finally discuss the challenges and opportunities for 2DEGs in RRAM applications.

Two-Dimensional Electron Gases Formed at Oxide Interfaces

The 2DEG formed in the oxide material system was first observed at the atomically sharp interface between epitaxial $LaAlO_3$ and single-crystalline $SrTiO_3$ substrates, each insulating on its own [1, 2] (**Figure 1A**). In parallel to significant research into the fundamentals of this rich 2D system [47–49], 2DEGs were reported in dozens of other oxide combinations, such as $GdTiO_3/SrTiO_3$ [50] and $NdTiO_3/SrTiO_3$ [51].

The origin of the 2DEG formed at the $LaAlO_3/SrTiO_3$ interface was initially ascribed to polar discontinuity, commonly referred to as the "polar catastrophe". The $LaAlO_3$

film consisting of charge-alternating planes of LaO^+ and AlO_2^- [52] is grown epitaxially on a TiO_2-terminated $SrTiO_3$ substrate. An electrostatic potential builds up in the $LaAlO_3$ layer and increases with its thickness. As the thickness of the $LaAlO_3$ film increases to four unit cells or higher, the voltage drop becomes sufficiently large for electrons to move from the surface of the $LaAlO_3$ film to the $LaAlO_3/SrTiO_3$ interface, where they occupy delocalized Ti 3d states in $SrTiO_3$ [52–56].

Besides the polar catastrophe mechanism, the ionic aspect of the interface plays an important role in its electronic properties [57]. Interdiffusion and intermixing of atoms across the interface [58] and oxygen vacancies [59–61] can account for the 2DEG formation via various ionic doping mechanisms. It is further argued that polar effects can drive such ionic mechanisms by making them more energetically favorable [62, 63]. These ionic features of the interface open opportunities to simplify the 2DEG material systems to non-polar, amorphous oxide materials. As such, the formation of 2DEG and their properties are strongly dependent on the material system, deposition method, and post-deposition processes.

The growth of epitaxial oxides requires slow and high-temperature (typically 650–900°C) processes using PLD or molecular-beam epitaxy (MBE). These features, and their low scalability (PLD), make the 2DEGs formed at epitaxial oxide interfaces incompatible with CMOS processes and large-scale fabrication. The use of amorphous oxide on single crystal oxide substrates [16, 24, 30, 31, 64–68] (**Figure 1B**) lowered the oxide deposition temperatures to <300°C and expanded the deposition methods to ALD. The use of amorphous oxides deposited on polycrystalline oxide [17, 21, 25, 32, 33, 69], which we term "All-ALD 2DEGs", provides a great advantage towards scalability and integration with existing and future technologies (**Figure 1C**). We note that significant progress has been demonstrated in MBE-based integration of epitaxial oxide 2DEGs systems with silicon [70–72] and other semiconductors [73, 74]. Still, while potentially scalable

[75], they remain slow, expensive, and high temperature (~600°C) and thus fall far behind the non-epitaxial ALD approaches.

This chronological trend of simplifying the materials and fabrication techniques has seen the transition from epitaxial interfaces (e.g., single crystalline $LaAlO_3$/single crystalline $SrTiO_3$, **Figure 1A**) to amorphous oxides on single-crystals (e.g., a-$LaAlO_3$/single crystalline $SrTiO_3$, **Figure 1B**), and recently to All-ALD 2DEGs with amorphous-polycrystalline systems (e.g., amorphous Al_2O_3/polycrystalline TiO_2, **Figure 1C**). The third system allows deposition temperatures to decrease to <300°C, well below the requirements of CMOS backend processes. Such advances hold the significant promise of realizing the potential of 2DEGs into practical devices and maturing them from single device lab-scale demonstrators towards scalable and microelectronics-compatible technology. In this mini review, we focus on the application of 2DEGs in RRAM devices.

Resistive Random-Access Memory Devices

The RRAM device has a simple metal-insulator-metal (MIM) structure with a resistive switching layer(s) sandwiched between two electrodes. It stores information by using different resistance states. For binary information storage, "0" and "1" information can be stored within one device cell using high and low resistance states (HRS and LRS, respectively). For multi-level information storage, more than a single bit of information can be stored within a single device cell using multiple resistance states. For example, information of "00", "01", "10", and "11" can be stored within one device cell using four different resistance states. Besides information storage, RRAM devices are also promising for new computing paradigms [39–44], which are faster in speed and lower in energy consumption. The resistive switching processes can accompany typical physical/chemical effects such as electrochemical/thermochemical reactions or metal-insulator transitions [34, 36, 40]. In the conductive filament (CF)-type RRAM devices, the mechanism of the resistance switching is the formation and disruption of conductive filaments (nanometric in diameter) within the resistive switching layer (a few nanometers in thickness) under external electrical stimuli. RRAM devices have many attractive features, such as small device area ($4 F^2$), fast switching speed (<1 ns) [76], high scalability [77–79], 3D integration capability [80, 81], and low energy consumption for resistance switching (<10 pJ/bit) [82, 83]. Based on the type of the conductive filaments, the RRAM devices can be divided into two types, which are the valence change memory (VCM) [76] and the electrochemical metallization memory (ECM) [84–86], which is also known as conductive-bridge RAM (CBRAM).

Two-Dimensional Electron Gases at Oxide Interfaces for Resistive Random-Access Memory Applications

Recently, 2DEGs have been leveraged for forming different types of RRAMs, by replacing one of the metal electrodes. This path can potentially increase design flexibility, enhance performance, and yield additional interesting properties.

In VCM devices, the 2DEG acts as an unconventional bottom electrode. In addition to the (electronic) conductivity of 2DEGs, their inherent ionic defects and instabilities can induce, interact with, and be utilized to control the resistive switching process. The oxide forming the 2DEG adjacent to the top electrode also acts as the resistive switching layer. The oxygen vacancies drift under the external electric field and create defect-induced gap states within the resistive switching layer during the resistive switching process. Whereas the electronic conduction property of 2DEGs performs as the function of a traditional metal bottom electrode. Several VCM RRAM devices have been recently reported, leveraging such 2DEG electrodes. These include Pt/$LaAlO_3$/$SrTiO_3$ [26], indium tin oxide (ITO)/$LaAlO_3$/$SrTiO_3$ [28], Pt/Ta_2O_{5-y}/Ta_2O_{5-x}/$SrTiO_3$ [27], and Pt/Al_2O_3/$SrTiO_3$ [24].

Wu et al. [26] were the first to use oxide 2DEGs in RRAM devices. Their device utilized the 2DEG formed at the epitaxial $LaAlO_3$/$SrTiO_3$ interface as the bottom electrode, the $LaAlO_3$ layer as the resistive switching layer, and the Pt layer as the top electrode layer. The conduction mechanisms are Ohmic transport at the low resistance state (LRS) and tunneling at the high resistance state (HRS). The $LaAlO_3$ layer was deposited on TiO_2-terminated $SrTiO_3$ (001) substrates using PLD at 800°C. The device switches based on the electric-field-induced drift of positively charged oxygen vacancies across the $LaAlO_3$/$SrTiO_3$ interface and the creation of defect-induced gap states within the ultrathin $LaAlO_3$ layer. Wu et al. [28] further substituted the Pt top electrode with ITO and demonstrated an optically transparent RRAM device. After replacing the Pt with ITO, the resistance window remained at 100. In contrast, the overall resistance level increased by five orders of magnitude from HRS at 10^4 Ω and LRS at 10^2 Ω to HRS at 10^9 and LRS at 10^7 Ω. The Pt/$LaAlO_3$/$SrTiO_3$ and ITO/$LaAlO_3$/$SrTiO_3$ structured devices both showed 2000 cycle endurance and 12 h retention, comparable to those in the Pt/$LaAlO_3$/Nb:$SrTiO_3$ structured devices [87].

Joung et al. [27] reported amorphous TaO_x/single crystal $SrTiO_3$ based VCM. Ta_2O_{5-y} (TO2)/Ta_2O_{5-x} (TO1) bilayer of TaO_x was deposited using PLD at 200°C under 70–100 mTorr oxygen (TO2) and at 700°C under 0.5 mTorr oxygen (TO1). The interface conductivity results from ionic defects formed during the high-temperature step and possibly kinetic damage from the PLD process. This use of amorphous layers constitutes progress toward simplifying the materials and deposition techniques. However, the PLD process's high temperature and low scalability remain incompatible with practical applications. The devices showed 2000 cycles endurance and 10^5 s retention. The best endurance and retention of TaO_x based RRAM devices are reported in Pt/$Ta_2O_{5-\delta}$/$TaO_{2-\beta}$/Pt structured devices [88] with 10^9 endurance cycles and 7.2×10^6 s retention.

Miron et al. [24] continued this trend of using amorphous layers for the 2DEG formation but focused on simple, low temperature, and scalable deposition. They reported amorphous Al_2O_3/single crystal $SrTiO_3$ based VCM devices, where the Al_2O_3 layer was deposited using ALD, with a low deposition temperature of 300°C (**Figure 2A**). The devices showed a large OFF/ON resistance ratio of ~10^6 and low operation currents down to 10^{-13} A (HRS,

FIGURE 2 | Recent examples of 2DEGs-based RRAM devices. **(A)** Schematic of a VCM-type RRAM device based on 2DEGs formed between amorphous ALD-Al_2O_3 and single-crystalline $SrTiO_3$ (STO) [24]. **(C)** Schematic of a CBRAM-type RRAM device based on the scalable All-ALD 2DEGs [25]. Panels **(B)** and **(D)** both present 100 cycles of consecutive DC current-voltage sweeps of the VCM and CBRAM devices (respectively).
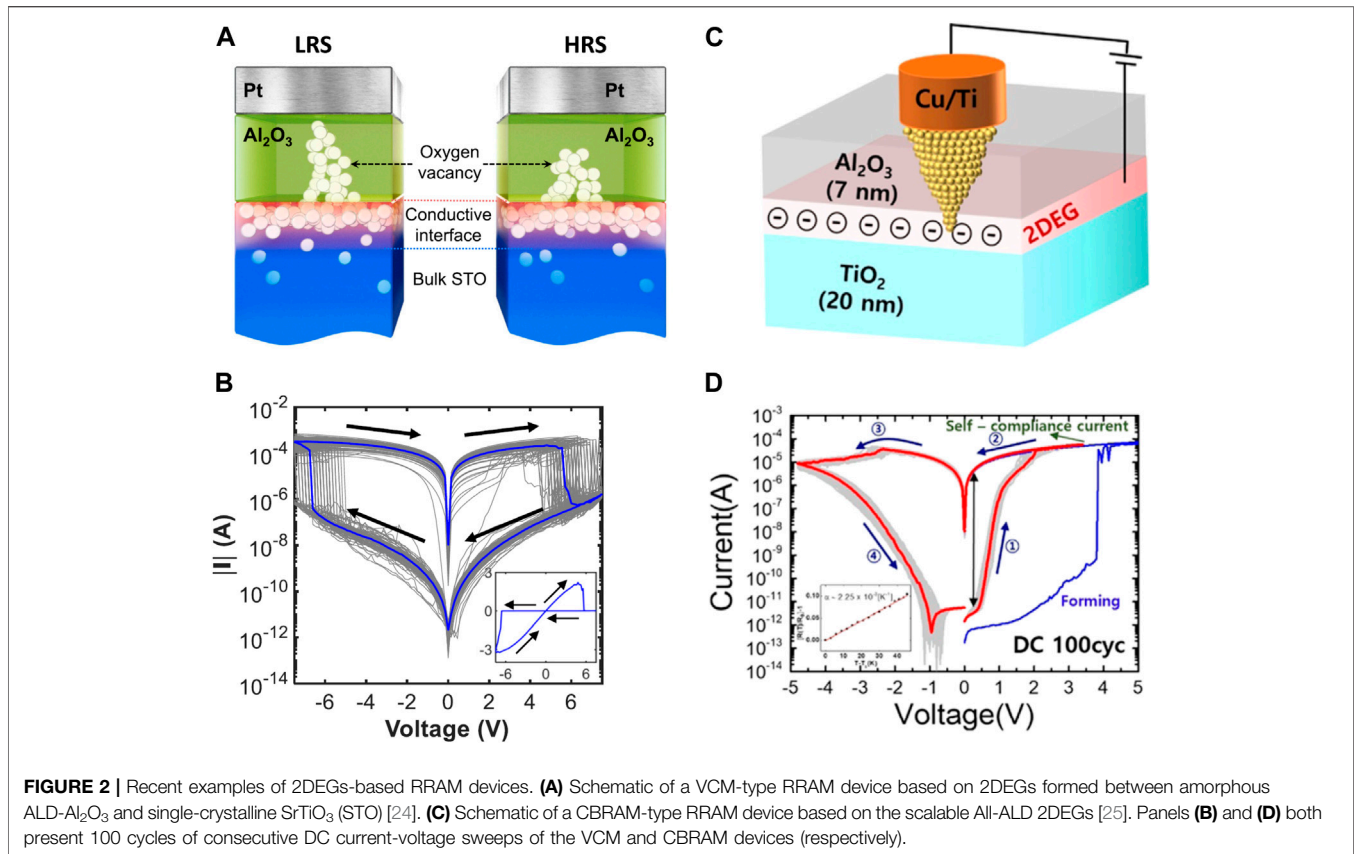
Figure 2B) with good cycle-to-cycle uniformity. The memory is based on the formation and rupture of oxygen vacancies filaments inside the Al_2O_3 layer. The oxygen vacancies driven from the interface into the insulating oxide under high electric fields are the key in enabling the resistive switching behavior. A key feature of this work is the application of low-defect Al_2O_3 [89], where the 2DEG serves as the bottom electrode and as the source of oxygen vacancies. The oxygen vacancies are injected by the electric field into the insulating Al_2O_3 to form the conductive filament. The practical consequence of this approach is the trigger of resistive switching behavior as compared to the $Pt/Al_2O_3/Nb:SrTiO_3$ stuctured device [89] and a large OFF/ON resistance ratio afforded by using a good insulator of Al_2O_3 as the resistive switching layer and the 2DEG as the bottom electrode [24, 90, 91]. The key shortcoming here was the large set/reset voltages, on the order of ± 7 V, another consequence of the insulating Al_2O_3. Further optimization of these devices, focusing on the insulator thickness, is expected to yield a better tradeoff between lowering the set/reset voltages while preserving the high OFF/ON resistance ratios.

As discussed earlier, All-ALD 2DEGs provide the most practical and scalable approach for 2DEG formation. Kim et al. [25] reported the first RRAM application of such 2DEGs, the only reported 2DEG CBRAM device (**Figures 2C,D**). They demonstrated a Cu conductive filament device based on 2DEG formed between amorphous Al_2O_3 and polycrystalline anatase TiO_2 (**Figure 1C**). Both materials were fabricated by ALD (250°C)

and, most importantly, without a crystalline substrate. The devices showed good endurance of 10^7 cycles and a high OFF/ ON resistance ratio of 10^6. Four different HRS levels are also achieved by adjusting the amplitude of the operation voltage pulses. The LRS kept constant, whereas the HRS increased as the device areas decreased. This resistance and device area dependency is beneficial for device area scaling. A higher OFF/ON resistance ratio and a lower current level can be achieved as the device area becomes smaller. The Cu conductive filament formed at LRS, observed by TEM, is about 20 nm in diameter. A device diameter of 20 nm is, in principle, the area scaling limit of such a device. This device also showed better endurance and retention behavior than $Cu/Al_2O_3/Pt$ structured devices [93, 94]. We highlight again the significant progress made by circumventing a single crystalline substrate, which allows integrating these devices on many substrates, such as the backend of silicon chips, flexible electronics [21], and others.

In more conventional VCM-type RRAM devices, the resistive-switching material typically contains some initial number of defects rearranged during the first forming process. A difference of 2DEGs-based VCM RRAM is that one can start with a fairly insulating material and use the 2DEG as *an extrinsic source of defects* [24]. This provides 2DEGs-based VCM RRAM with significantly larger OFF/ON resistance ratios compared to more conventional approaches. The high OFF/ON resistance ratio offers potential for multi-level resistance operation. The

TABLE 1 | Comparison of device performances.

Device Structure	Device Size	Forming (Yes/No, $V_{forming}$, Icc)	Top electrode	Resistive switching layer	Bottom electrode	Switching polarity	SET/RESET Voltage (DC)	Max Iset/I_{CC} (DC)	Max Ireset (DC)	SET/RESET Voltage (AC)	SET/RESET Switching speed (AC)	HRS/LRS (Ω)	Resistance ratio	Endurance (cycles)	Retention (s)
Pt/LaAlO$_3$/SrTiO$_3$ [26]	2.25×10^4 μm²	Yes, -4 V, 30 mA	Pt	LaAlO$_3$	LaAlO$_3$/SrTiO$_3$ 2DEG	bipolar	−4 V/+4 V	30 mA/No I_{CC}	30 mA	−4 V/+4 V −4 V/+9 V	5 ns/100 μs 5 ns/1 μs	10^4/10^2	10^2	2000	>4.32 × 10^3 (@25°C)
ITO/ LaAlO$_3$/ SrTiO$_3$ [28]	9×10^4 μm²	Yes, -3.3 V, 30 μA	ITO	LaAlO$_3$	LaAlO$_3$/ SrTiO$_3$ 2DEG	bipolar	−1.5 V/+5 V	30 μA/No I_{CC}	0.5 nA	−5 V/+5 V	Not given	10^9/10^7	10^2	2000	>4 × 10^4 (@25°C)
Pt/LaAlO$_3$/ Nb: SrTiO$_3$ [87]	10^6 to 10^4 μm²	Yes, -13 to -40 V (P$_{O2}$ and t$_{ox}$ dependent), I_{CC} not given	Pt	LaAlO$_3$	Nb: SrTiO$_3$	bipolar	−6 V/+6 V	70 mA/no I_{CC}	10 mA	−8 V/+8 V	Not given	10^6/10^3	10^3	2000	>4.32 × 10^3 (@25°C)
ITO/ LaAlO$_3$/ ITO [94]	1.13×10^6 μm² (ø = 1,200 μm)	Yes, -1 V to -2.6 V (P$_{O2}$ dependent), 10 mA	ITO	LaAlO$_3$	ITO	bipolar	Not given/+3 V	Not given	5–10 mA	Not given	Not given	10^3/10^2	10	100	Not given
Pt/Ta$_2$O$_{5-y}$/ Ta$_2$O$_{5-x}$/ STO [27]	490.63 μm² (ø = 25 μm)	Not mentioned	Pt	Ta$_2$O$_{5-y}$	Ta$_2$O$_{5-x}$/ STO 2DEG	bipolar	+4 V/−2.5 V	2 μA/no I_{CC}	1 μA	Not given	Not given	10^{12}/10^8	10^4	2,900	>10^5 (@25°C)
Pt/Ta$_2$O$_{5-δ}$/TaO$_{2-β}$/Pt [88]	0.25 μm²	Not mentioned	Pt	Ta$_2$O$_{5-δ}$/TaO$_{2-β}$	Pt	bipolar	−0.9 V/+2 V	170 μA/ 170 μA	170 μA	2 V/−1.5 V	10 ns	10^3/10^2	10	10^9	1.08 × 10^7 (@150°C)
Pt/Al$_2$O$_3$/ STO [24] Pt/Al$_2$O$_3$/ Nb: SrTiO$_3$ [89]	2.7×10^4 to 1.5×10^5 μm² No resistive switching behavior	Yes, -6 V to −4 V, 0.1 mA	Pt	Al$_2$O$_3$	Al$_2$O$_3$/STO 2DEG	bipolar	−7 V/+7 V	0.5 mA/not mentioned	0.5 mA	Not given	Not given	10^{10}/10^4	10^6	100	Not Given
Pt/Al$_2$O$_3$/ TiN [90]	2.5×10^{-3} μm²	Yes, 7 V, <10 μA, no I_{CC}	Pt	Al$_2$O$_3$	TiN	Bipolar	+3 V/−2 V	<300 μA/ 300 μA	<1 mA	8 V/−4 V	10 ns/10 ns	10^6/10^3	10^3	1,000	Not given
Ni/Al$_2$O$_3$/ Pt [90]	10^4 μm²	Yes, 5 V, 500 μA	Ni	Al$_2$O$_3$	Pt	Bipolar	+1.2 V/ −0.45 V to −0.6 V	500 μA/ 500 μA	<2 mA	1.5 V/−0.4 V to −0.58 V	5 ms/5 ms	2.8 × 10^3 to 2.2 × 10^3/470	6 to 4.7	100	10_3 s
Cu/Al$_2$O$_3$/ TiO$_2$ [25]	0.02–340 μm²	Yes, 1 to 5V, no Icc (self-compliance), I_{max}<0.1 mA	Cu	Al$_2$O$_3$	Al$_2$O$_3$/TiO$_2$ 2DEG	bipolar	+3 V/−5 V	<0.1 mA/no I_{CC} (self-compliance)	<0.1 mA	Not given	500–800 ns	10^{11}/10^5	10^6	10^7	10^6 (@85°C)
Cu/Al$_2$O$_3$/ Pt [92]	3.14×10^4 μm² (ø = 200 μm)	Yes, 8 V, 200 μA	Cu	Al$_2$O$_3$	Pt	bipolar	0.3–1.2 V/-0.1 V to −0.7 V	150 μA/ 150 μA	<0.1 mA	Not given	Not given	10^9/10^3	10^6	2000	10^5
Cu/Ti/ Al$_2$O$_3$/ Pt [93]	0.05 μm² (via hole ø = 0.25 μm)	Yes, 1.1 V, 200 μA	Cu/Ti	Al$_2$O$_3$	Pt	bipolar	0.3–0.7 V/ −0.1 V to −0.3 V	200 μA/ 200 μA	~0.1 mA	Not given	Not given	10^9/10^4	10^5	Not given	10^4
Pt/WO$_x$/ W [96]	2×10^{-3} μm²	No, Forming free	Pt	WO$_x$	W	bipolar	1 V/−1 V	4 mA/no I_{CC}	<0.2 mA	+1.25 V/-1 V	5 μs/5 μs	10^6/10^4	10^2	10^7	Not Given
IrO$_x$/Al$_2$O$_3$/ TiO$_x$/ TiN [97]	0.24 μm²	Yes, 7.5–20 V, 100 μA	IrO$_x$	Al$_2$O$_3$ (2–8 nm)/ TiO$_x$	TiN	bipolar	3.5–5.4 V/ −3 V	100 μA/ 100 μA	<15 μA	+3 V–5.5 V/- 3 V	500 μs/ 10 ms	4 × 10^6 to 10^7/ 0.4 × 10^6 to 10^6 to	10.8 to 21.62	10^5 to 10^6	Not Given

TABLE 1 | (Continued) Comparison of device performances.

Device Structure	Device Size	Forming (Yes/No, $V_{forming}$, Icc)	Top electrode	Resistive switching layer	Bottom electrode	Switching polarity	SET/RESET Voltage (DC)	Max Iset/Icc (DC)	Max Ireset (DC)	SET/RESET Voltage (AC)	SET/RESET Switching speed (AC)	HRS/LRS (Ω)	Resistance ratio	Endurance (cycles)	Retention (s)
TiN/Ti/TiO$_{2-x}$/TiO$_{2-y}$/Au [98]	10^4 μm²	No, Forming free	TiN/Ti	TiO$_{2-x}$/TiO$_{2-y}$	Au	bipolar	3 V/-3 V	<0.1 mA/No Icc (self-compliance)	<0.1 μA	+8 V/-8 V	10 ms/10 ms	1.2×10^6	2 to 3.6×10³	Not Given	Not Given
Ru/TiO$_{2-x}$/HfO$_2$/Ru [99]	10^4 μm²	Yes, 4-4.5 V, 5 mA	Ru	TiO$_{2-x}$/HfO$_2$	Ru	bipolar	2 V/-1.5 V	5 mA/5 mA	<5 mA	Not given	Not given	8×10^8 to 4×10^{10}/6×10^5 to 5×10^8	10	10^4	10^5
Ni/GeO/SrTiO$_3$/TaN [100]	11304 μm²	Not given	Ni	GeO/SrTiO$_3$	TaN	bipolar	-0.3 V to -1.2 V/ 0.13-0.3 V	3.5 μA/No Icc (self-compliance)	0.12 nA	-1.5 V/0.5 V	50 ns/50 ns	$10^3/10^2$ $10^{12}/10^6$	10^6	10^6	4×10^5 @85°C

broader ratio provides more room for improvement of this feature, as more distinct states can fit this wider resistivity range [94]. However, multi-level behavior has yet to be reported in 2DEGs based VCM devices due to the abruptness of their switching. Another consequence of the high OFF/ON resistance ratio is extremely low current at HRS, which benefits low-power operation. A comparison of 2DEG based RRAM devices, devices that show close similarity to the 2DEG based device structures, and some other RRAM devices are listed in **Table 1**.

We consider the progress made with the All-ALD 2DEGs [25, 33] to be a defining point. The All-ALD 2DEGs have liberated 2DEGs from small and expensive single-crystal substrates and from costly high-temperature fabrication processes. 2DEGs are now being fabricated by ALD on many substrates while keeping a low thermal budget and using low-cost, highly scalable, mature, and microelectronics-compatible techniques. The use of anatase TiO$_2$ provides another advantage of a potentially more conductive 2DEG compared to the LaAlO$_3$/SrTiO$_3$ interface at room temperature [64] and offers tunability of the conductivity [32, 33]. Higher conductivity of the 2DEG is desirable in RRAM applications because the resistance of the bottom electrode is in series with the resistive switching layer, making lower resistance beneficial for stabilizing the resistive switching behavior, and for reducing the operating power. These issues become more important when considering integrating devices into a crossbar structure.

CHALLENGES

The 2DEGs based RRAM devices reported so far are all single device demonstrations. Integration of the 2DEGs based RRAM devices into a crossbar array or 3D vertical structures poses an open challenge, which requires several issues to be addressed. Due to their high series resistance, the relatively high sheet resistance of many 2DEGs (typically >10^4 Ω/□) makes it challenging to utilize 2DEGs as thin line bottom electrodes. Beyond increasing the operating voltage (and power), this series resistance of the bottom electrode could further cause a significant spatial distribution of operation voltages across a crossbar array. As such, it remains an important task to reduce the 2DEG resistivity and design new device structures for high-density RRAM integration. Another facet of these challenges is microfabrication: 2DEGs, particularly those driven by defects, can be challenging to pattern efficiently [101–103]. Robust fabrication techniques need to be designed to produce the small features necessary for high-density RRAM arrays. In addition, further flexibility in the tuning of the 2DEG resistivity would provide an advantage for device and array optimization, which would further benefit from a deeper understanding of the 2DEGs-based RRAM switching mechanisms.

OPPORTUNITIES

As discussed earlier, 2DEGs-based RRAMs can feature large, potentially tunable OFF/ON resistance ratios. These provide

prospects of low power operation, allow additional "room" for efficient multi-level resistance states, and provide additional design flexibility and tunability compared to some of the current devices. The 2DEGs-based VCM devices so far all showed abrupt switching processes, resulting in binary resistance states. Further development of these devices into multi-level capabilities will provide considerable functionality benefits. Since 2DEGs are successfully applied as the channel of transistors [15, 16, 19, 32]. This opens routes for integrating both the memory and the peripheral circuits within the same material system and even within the same lithography process steps. This is also a very attractive feature for RRAM devices in crossbar arrays since the crossbar structured RRAM devices require selectors to select different rows and columns.

AUTHOR CONTRIBUTIONS

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