Resistive switching devices herald a transformative technology for memory and computation, offering considerable advantages in performance and energy efficiency. Here, a simple and scalable material system of conductive oxide interfaces is employed, and their unique properties are leveraged for a new type of resistive switching device. An Al₂O₃–TiO₂-based valence-change resistive switching device, where the conductive oxide interface serves both as the bottom electrode and as a reservoir of defects for switching, is demonstrated. The amorphous–polycrystalline Al₂O₃–TiO₂ conductive interface is obtained following the technological path of simplifying the fabrication of the 2D electron gases (2DEGs), making them scalable for practical mass integration. Physical analysis of the device chemistry and microstructure with comprehensive electrical analysis of its switching behavior and performance is combined. The origin of the resistive switching is pinpointed to the conductive oxide interface, which serves both as the bottom electrode and as a reservoir of oxygen vacancies. The latter plays a key role in valence-change resistive switching devices. The new device, based on scalable and complementary metal–oxide–semiconductor (CMOS)-technology-compatible fabrication processes, opens new design spaces toward increased tunability and simplification of the device selection challenge.

1. Introduction

The 2D electron gases (2DEGs) formed at some oxide interfaces provide a fertile ground for many physical phenomena [1–6]. The 2DEG make it interesting for various device applications such as the channel in transistors [7–9] and the electrode in resistive switching memories [10–14]. Resistive switching memories, which have a metal–oxide–metal sandwich structure, are promising candidates for next-generation memories to address the vast data storage requirement in the big data era [15,16]. Its conductance tunability emulating the synaptic plasticity makes it applicable for brain-inspired in-memory computing [17–20] which can overcome the memory bottleneck in the traditional von Neumann architecture and drastically decrease the energy consumption.

Several 2DEGs based valence change memory (VCM) devices were reported on various materials systems [10,12–14] which share a common feature of using single-crystal SrTiO₃ substrates. The 2DEGs in these works function as the bottom electrodes of the devices. Originally, 2DEGs were fabricated exclusively by oxide epitaxy, typically by pulsed laser deposition (PLD) at high temperatures of 600–800 °C. The epitaxial oxide layer was subsequently replaced by amorphous oxides, such as Al₂O₃, which lowered the deposition temperature to ~300 °C by the use of atomic layer deposition (ALD) [21]. However, the use of SrTiO₃ single crystal substrates hinders the scalability and makes direct integration of such devices too complicated for the complementary metal–oxide–semiconductor (CMOS) process. Recent works have reported 2DEG at the interface of amorphous Al₂O₃ and polycrystalline TiO₂ [8,11,22–24] both deposited in a single ALD process. The mechanism of the 2DEG formation was determined to be the formation of oxygen vacancies at the TiO₂ surface through a reduction caused by the Al ALD precursor in the initial stages of Al₂O₃ deposition [21]. These negative charges at the TiO₂ side of the interface result in a downward band bending at the TiO₂ surface, which was shown to localize the 2DEG carriers near the interface [20]. The use of low-temperature ALD opens the opportunity for scalable fabrication of resistive switching memory devices with CMOS-compatible processes and materials that can be integrated on the Si backend or a variety of other substrates. An electrochemical metallization (ECM) device of Cu/Ti/Al₂O₃/TiO₂ has been reported [11] where the resistive switching is based on the formation and rupture of filaments that do not exist in the corresponding bulk oxide materials. These phenomena and the sheet resistance tunability of the 2DEG make it interesting for various device applications such as the channel in transistors [7–9] and the electrode in resistive switching memories [10–14].

Reservoirs for Resistive Switching Devices

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consisting of Cu metal ions from the top electrode. The 2DEG formed at the Al$_2$O$_3$/TiO$_2$ interface is inherently driven by oxygen vacancies, and it can thus act as an oxygen vacancy reservoir for VCM type resistive switching memory devices in addition to its more conventional role as a bottom electrode.

Here we report the first demonstration of VCM devices based on the 2DEGs formed at the Al$_2$O$_3$/TiO$_2$ interface. The interface is fabricated at low temperatures (<300 °C) using the scalable ALD technique. The use of the low-temperature ALD and simple binary oxide materials system provides a unique feature of the 2DEG based devices being able to be integrated with the back-end-of-line CMOS process. Note that for the sake of convenience, we use the term 2DEG very loosely to describe conductive oxide interfaces, in many of which the conductivity is not limited to a 2D sheet exactly at the interface, and it may extend deeper into the bottom material.

Unlike standard resistive switching devices, where the bottom electrode is a metal, a distinct feature of the 2DEG electrode is that it can be switched off, via depletion by field effect.[8] This feature of 2DEGs opens prospects of depleting the device’s bottom electrode via the top electrode, which would result in a strongly asymmetric behavior. The asymmetry provides the potential to design self-rectifying resistive switching devices.[36-45] This is an attractive approach for inhibiting sneak-path currents, which circumvents the necessity of additional transistors or selector devices in cross-bar arrays.[36] As such, self-rectifying devices can dramatically simplify the large-scale integration of resistive switching memory arrays.

Our demonstration of scalable 2DEG-based VCM devices paves the way toward fulfilling this promise.

2. Results and Discussion

We start by understanding the 2DEGs’ features and mechanism and then follow on their role in the device.

2.1. Conductive Interface between Al$_2$O$_3$ and TiO$_2$

The Al$_2$O$_3$/TiO$_2$ 2DEG sheet resistance is determined as 5000 ± 40 Ω square$^{-1}$ using the Van der Pauw configuration. The substrate is connected in parallel to the 2DEG, but it does not significantly affect the 2DEG’s role in the resistive switching given its high resistivity (≈70 kΩ) and vertical distance (SiO$_2$+TiO$_2$ layers) from the resistive switching layer, Al$_2$O$_3$. The cross-sectional transmission electron microscopy (TEM) image of the Al$_2$O$_3$/TiO$_2$ heterostructure is shown in Figure 1a. The phase contrast from the TiO$_2$ layer indicates that it is primarily polycrystalline. The crystal structure of TiO$_2$ is determined as anatase as indicated by grazing-incidence X-ray diffraction (GIXRD, Figure 1b, ICDD card #00-21-1272), and the thickness is 14.8 ± 0.6 nm determined by X-ray reflectivity (XRR, Figure S1, Supporting Information). No phase contrast or a clear crystal lattice is observed in the TEM image of the Al$_2$O$_3$ layer. Our prior diffraction results[27] have shown the Al$_2$O$_3$ layer to be amorphous.
The mechanism behind the interface conductivity is probed by X-ray photoelectron spectroscopy (XPS) analysis of the Ti 2p region in TiO₂ (Figure 1c,d). A spectrum of the surface of the unapped TiO₂ (also 14.8 ± 0.6 nm thick, without an Al₂O₃ over-layer) shows a nearly stoichiometric Ti⁴⁺ originating in TiO₂ (Figure 1c). A similar sample with a 2 nm thick Al₂O₃ capping layer shows a significant Ti⁵⁺ component, constituting 15 ± 0.5% of the Ti 2p total peak area (Figure 1d). This lower oxidation state results from a reduction of the TiO₂ by the Al precursor during the early stages of the ALD-Al₂O₃ process,[23] leading to the generation of oxygen vacancies. These oxygen vacancies act as n-type dopants in the otherwise insulating TiO₂, and they are therefore the source of the 2DEG.[8] This XPS fingerprint of 2DEG formation is also commonly observed in 2DEGs based on SrTiO₃ substrates.[21,28–30] Samples without the Al₂O₃ layer, showing no Ti⁵⁺ features (Figure 1c), are electrically insulating ($R_\text{g}$ > 10⁹ Ω square⁻¹, out of our test equipment limit), showing only negligible contribution of conductivity from the Si substrate below (or no measurable conductivity when deposited on a glass substrate for comparison).

Therefore, the process described here for Al₂O₃ deposition results in the formation of 2DEGs at the Al₂O₃/TiO₂ interface, as observed by the interface conductivity and the significant Ti⁵⁺ component (Figure 1d). These observations reproduce the results of Seok et al. who showed that the conductivity originates from interfacial oxygen vacancies[30] generated during the Al₂O₃ deposition.[21]

Here the Al₂O₃ (2 nm) acts as a protection layer for the 2DEG formed in the surface of TiO₂.[20] It was intentionally made thin to allow the XPS to probe the underlying TiO₂, whereas, in the device to follow, thicker Al₂O₃ layers (5 nm) will be employed. The reduction process may well extend the range of the oxygen vacancies into the TiO₂ layer, making the conductivity not limited strictly to the Al₂O₃/TiO₂ interface. Therefore, the use of the term 2DEG is not rigorously justified, rather it is used here loosely for convenience.[11]

2.2. 2DEG-Based VCM Devices

Having set the ground with the analysis of the 2DEGs, we then fabricate VCM devices from Pt (50 nm)/Al₂O₃ (5 nm)/TiO₂ (14.8 nm) structures. The Pt layer acts as the top electrode, and the Al₂O₃ layer acts as the resistive switching layer. The conductive 2DEG at the Al₂O₃/TiO₂ interface acts as the bottom electrode and as the oxygen vacancies reservoir for the VCM device here. The 2DEG electrode is contacted with contacts at the corners of the sample (Figure 2a).

When operating the device, we apply the voltage on the Pt top electrode and ground the 2DEG bottom electrode (Figure 2a). After the initial forming process, subsequent transitions from high resistance state (HRS) to low resistance state (LRS) are defined as SET, and the reverse process as RESET. The compliance currents used in the forming and the SET process are set to 10⁻⁴ A. The $I$–$V$ curves of the forming cycle and a typical switching cycle are shown in Figure 2b. Five different devices are tested under DC mode using voltage sweeps, and each device is switched for 20 cycles after the forming process (Figure 2c). All five devices exhibit comparable behavior and low device-to-device variability. The detailed switching parameters are provided in Figure S2 (Supporting Information).

In addition to the 2DEG’s role as the bottom electrode, it further functions as the source of oxygen vacancies responsible for the resistive switching behavior of the Al₂O₃ layer. In a previous work, we deposited Al₂O₃ layers with an identical recipe on conductive Nb:SrTiO₃ layers, where no interface vacancies were formed. These structures exhibit robust insulting properties, and no hysteresis behavior.[12] The key difference from the current case is the reduction of the TiO₂ surface, allowing us to pinpoint the interface as the source of vacancies for resistive switching, which are injected (forming) into the Al₂O₃ layer.[13] This differs from typical memristors where the resistive switching layer is intentionally enriched with defects, whereas our approach allows the use of an initially low-defect and

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**Figure 2.** The Pt/Al₂O₃/TiO₂ device structure and DC mode resistive switching $I$–$V$ curves. a) Schematic illustration of the device structure with the 2DEG acting as the bottom electrode. The Pt acts as the top electrode and the Al₂O₃ acts as the resistive switching layer. The voltage is always applied to the Pt top electrode, and the 2DEG is always grounded during the tests. Oxygen vacancies are schematically denoted by circles. b) $I$–$V$ curves of a forming cycle and a typical switching cycle in DC mode. The forming, SET, and RESET points are noted on the curves. The annotations of ① ② ③ ④ ⑤ show the sequence of the voltage sweep and the arrows show the voltage sweep direction. c) $I$–$V$ curves of five devices. The red lines are the forming cycles. The blue lines represent the typical resistive switching cycles. The gray lines correspond to all $I$–$V$ cycles after the forming cycles.
insulating Al$_2$O$_3$, which heralds a memory window of $\approx 4$ orders of magnitude at $\pm 0.2$ V. Since the insulating Al$_2$O$_3$ layer is connected in series with the 2DEG (Figure 1a), the LRS resistance can only be explained by modulation of the Al$_2$O$_3$ resistance, to be further discussed on Section 2.3.

The retention of HRS and LRS are tested at room temperature using 0.1 V read voltage. Both resistance states remain stable for $10^4$ s without degradation (Figure S3a, Supporting Information), which is comparable to other 2DEG based VCM devices on SrTiO$_3$ substrates.$^{[10,12,14]}$ At $80 \, ^\circ$C and 0.1 V the LRS and HRS showed stability for $10^3$ s, after which instabilities occur leading to breakdown (Figure S3b, Supporting Information).

In addition to DC switching analysis, the endurance of the devices is tested under pulsed switching using 100 $\mu$s width voltage pulses (Figure 3). The resistance window is set to be $10$, with the LRS lower than $10^6$ $\Omega$ and the HRS higher than $10^7$ $\Omega$ (Figure 3a). An operate-and-verify programming scheme$^{[33–36]}$ is used here, which means more than a single pulse may be used in the SET or RESET operations. The voltage height in both SET and RESET will increase until the resistance is tuned to the destination resistance value. The details of the operate-and-verify programming scheme are shown in Figures S4–S6 (Supporting Information). The reason for using the operate-and-verify programming scheme is that the device might not reach the desired resistance range after a single pulse operation. To ensure the device’s resistance is indeed programmed to the desired value, a verification step is necessary. This operate-and-verify programming scheme requires higher energy consumption compared to single-pulse programming scheme, but it is more reliable and it guarantees the resistance modulation success for each cycle. All the HRS and LRS in both DC mode and pulse mode are read at a voltage of 0.1 V. Due to the intrinsic stochastic nature of the devices’ switching process which includes the formation and rupture of the conductive filament (CF), the devices exhibit cycle-to-cycle variation (Figure 3a). The LRS values vary from 77 k$\Omega$ to 1 M$\Omega$ and follow a normal distribution ($\mu = 7.2 \times 10^5$, $\sigma = 2.1 \times 10^5$). The HRS vary from 10 M$\Omega$ to 87 G$\Omega$ and follow a lognormal distribution (Figure 3b). The resistances of the device show no observable degradation after $10^3$ cycles of operation.

About 98% of the RESET cycles require no more than 2 pulses to switch the device from HRS to LRS, and about 85% of the SET cycles require no more than 3 pulses to switching the device from LRS to HRS (Figure 3c,d). The SET voltage and the number of pulses required to switch the device from HRS to LRS increase as the cycle number increases (Figure 3c), indicating that further engineering will be necessary to mature these devices for practical applications.

### 2.3. Switching Mechanism

The resistive switching behavior of the Pt/Al$_2$O$_3$/TiO$_2$ VCM devices can be explained by the formation and partial rupture of the CFs consisting of oxygen vacancies$^{[20,37–40]}$ inside the Al$_2$O$_3$ layer, as illustrated in Figure 4.
The pristine device starts with no CFs inside the Al₂O₃ layer (Figure 4a). During the forming process, an external negative voltage is applied to the Pt electrode and the positively charged oxygen vacancies migrate toward the top electrode which leads to the formation of CF consisting of oxygen vacancies (Figure 4b,c). The device switches from initial high resistance state to low resistance state.

In the RESET process, a positive voltage is applied to the Pt top electrode and the bottom electrode is grounded. The oxygen vacancies migrate toward the bottom electrode and the gap length \( \Delta \) between the remnant CF grows, which leads to the rupture of CF (Figure 4c–e). The device switches from LRS to HRS. We note that the unconventional use of a highly insulating Al₂O₃ is the key here to obtaining the large memory window by increasing the resistance at HRS.

In the SET process, a negative voltage is applied to the top electrode and the bottom electrode is grounded. At first, the length of the gap \( \Delta \) decreases until the partial filament forms a continuous filament connecting the top and the bottom electrode (Figure 4e,f). Only after the continuous CF forms, the diameter \( \phi \) increases only after a continuous CF is formed.

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The use of the Si substrate and simple binary oxide materials of Al₂O₃ and TiO₂ demonstrate the feasibility of integrating 2DEG into Si-based and CMOS-compatible devices. The ability to deplete the 2DEGs provides a route toward self-rectifying devices, and the possibility of replacing the top metal electrode with a transparent oxide electrode further allows the device to be extended to wider applications.
4. Experimental Section

The substrates used are (100) n-type unintentionally doped Si (MTI Corp., resistivity = 70k Ω cm) with ~2 nm native SiO₂. The TiO₂ films are deposited on the substrates by ALD (ULtratech/Cambridge Nanotech Fiji G2) at 250 °C using tetrakis(dimethylamido)titanium (TDMAT) and Ar₂O (4:1) plasma as the Ti and oxygen precursors, respectively. The TDMAT is heated to 75 °C in the bubbler and introduced to the ALD reactor by 30 sccm of Ar carrier gas. The TiO₂ deposition sequence consists of TDMAT injection (0.025 s)/purge (10 s)/Ar₂O plasma (5 s)/purge (5 s). The samples are kept inside the ALD chamber under vacuum (~2 x 10⁻² Torr) after the TiO₂ deposition. The temperature is increased from 250 to 300 °C and stabilized at 300 °C, taking 15 min altogether. This step was found to be important for reducing the sheet resistance. Subsequently, 10 trimethylaluminum (TMA) reducing pulses (0.1 s pulse duration) are injected into the chamber prior to Al₂O₃ deposition. Finally, 2 nm (for XPS characterization) or 5 nm (for device testing) Al₂O₃ thin films are deposited on the TiO₂ at 300 °C. TMA and H₂O are used as the Al and oxygen precursors, respectively. The Al₂O₃ deposition sequence consists of TMA injection (0.1 s)/purge (10 s)/H₂O (0.3 s)/purge (5 s). Pt top electrodes (50 nm thick) are deposited on top of the Al₂O₃ layer through a shadow mask with a diameter of 120 μm using e-beam deposition. Contacts to the 2DEG are done by scratching the samples’ corners from the top of the samples’ surface following depositing a layer of 50 nm thick Al by e-beam deposition (Evatec BAK-501A) at room temperature on the surface of the samples’ edges.

Cross-sectional specimens were prepared through a conventional TEM sample preparation routine. Starting with cutting and gluing, the TEM specimens are then ground, planar parallel polished, and further perforated and electron transparent thin area with a Gatan Precision Ion Polishing System (PIPS II 695, Gatan Inc.). The microstructure is characterized by FEI Tecnai F30 analytical TEM operating at 300 kV. Ion Polishing System (PIPS II 695, Gatan Inc.). The microstructure is characterized by FEI Tecnai F30 analytical TEM operating at 300 kV. The films’ crystallinity is analyzed by GIXRD, and the film’s thickness is analyzed by XRR using Rigaku SmartLab diffractometer. The GIXRD incident angle is 0.5°. The sample are mounted on zero-diffraction discs (MTI Corp.) during the test.

XPS measurements are performed in ultrahigh vacuum (2.5 x 10⁻¹⁰ Torr base pressure) using the 5600 Multi-Technique System (PHI, USA). The samples are irradiated with an Al Kα monochromated source (1486.6 eV), and the electrons are analyzed by a Spherical Capacitor Analyzer using a slit aperture of 0.8 mm. All spectra are shifted to align the adventitious C1s peak at 284.8 eV.

The sheet resistance of the 2DEG is measured using the Van der Pauw configuration at room temperature. The sheet resistance and DC device analysis is done using a light-sealed probe station with a Keithley Pauw configuration at room temperature. The sheet resistance and DC device analysis is done using a light-sealed probe station with a Keithley Pauw configuration at room temperature. The sheet resistance and DC device analysis is done using a light-sealed probe station with a Keithley Pauw configuration at room temperature. The sheet resistance and DC device analysis is done using a light-sealed probe station with a Keithley Pauw configuration at room temperature.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

The authors are grateful for the support of the Israeli Science Foundation (ISF Grant No. 375/17). Partial support in the fabrication and characterization of the samples was provided by the Technion’s Micro-Nano Fabrication & Printing Unit (MNF&PU) and the Russell Berrie Nanotechnology Institute (RBNI). The authors would like to thank the assistance and support from Dr. Kamira Weinfeld and Dr. Pini Shketer for XPS characterization, Valentina Korchnoy for ALD, Arkadi Gavrilov for e-beam evaporation, and Dr. Maria Kolman Kristosov for XRD characterization. Y.L. acknowledges partial support from a Technion Fellowship. K.W. was supported in part at the Technion by the Aly Kaufman Fellowship. The work at Los Alamos National Laboratory was supported by the NNSA’s Laboratory Directed Research and Development Program, and was performed, in part, at the CINT, an Office of Science User Facility operated for the U.S. Department of Energy Office of Science. Los Alamos National Laboratory, an affirmitive action-equal opportunity employer, is managed by Triad National Security, LLC for the U.S. Department of Energy’s NNSA, under Contract No. 89233218CNA000001.

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The raw data used to prepare the figures in this work is available in an annotatedxlsx file in the Supporting Information.

Keywords

atomic layer deposition, conductive oxide interfaces, resistive switching, resistive switching memory, 2D electron gas, valence change memory

Received: July 17, 2022
Revised: September 29, 2022
Published online:
