ADVANCED ELECTRONIC MATERIALS

Supporting Information

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Scalable Al_2O_3–TiO_2 Conductive Oxide Interfaces as Defect Reservoirs for Resistive Switching Devices

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Supplementary Information for:
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The TiO_2 film thicknesses are determined by using x-ray reflectometry (XRR, Figure S1).

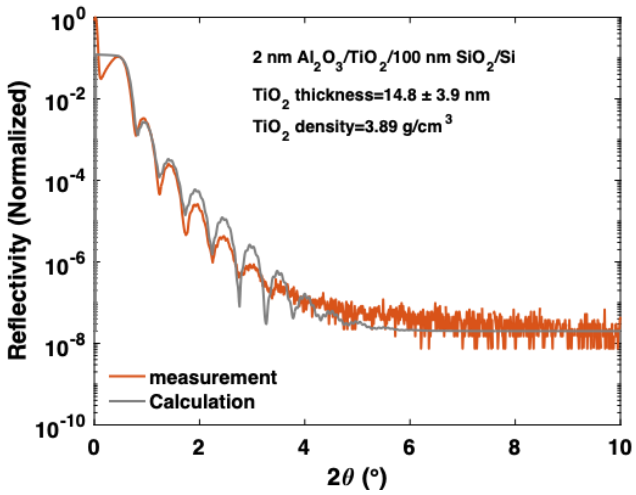


Figure S1. X-ray reflectometry (XRR) of the 2 nm Al_2O_3/TiO_2/native SiO_2/Si film stacks. The thickness of the TiO_2 was calculated to be 14.8 ± 0.6 nm using the TiO_2 film density of 3.89 $g \cdot cm^{-3}$.

The XPS spectra are fitted using the CasaXPS software with a Shirley background and a Lorentzian-Gaussian line shape with a ratio of 30%. During the XPS data analysis, the Ti 2p 3/2 peak and Ti 2p 1/2 peak area ratio is fixed to 0.5. The XPS spectra are modeled using the parameters listed in Table S 1. The peak positions and full width at half maximum (FWHM) are similar to the reference. [1]

Table S1. The binding energies and full width at half maximum (FWHM) of Ti oxidation states.

Oxide State	Binding Energy (eV)					
	Uncapped TiO_2		TiO_2/Al_2O_3		D. Gonbeau et al.[1]	
	Peak position [eV]	FWHM [eV]	Peak position [eV]	FWHM [eV]	Peak position [eV]	FWHM [eV]
Ti^{4+} 2p 3/2	458.32	0.95	458.29	1.04	458.7	1.5
Ti^{3+} 2p 3/2	--	--	456.82	1.88	456.6	1.4

DC and AC resistive switching mode

A forming process, which is usually conducted in DC mode, is required to trigger the resistive switching behavior of the device. In the forming process, the voltage sweeps forward from 0 V to -6 V (red line annotated by ① in Figure 2b) and backward from -6 V to 0 V (red line annotated by ② in Figure 2b), i.e., the double voltage sweep between 0 V and -6 V, with a compliance current of 10^{-4} A. The forming process switches the device resistance from the initial high resistance state (HRS) to low resistance state (LRS) and leads to the formation of conductive filaments (CFs) that are consist of oxygen vacancies [2] inside the Al_2O_3 layer.

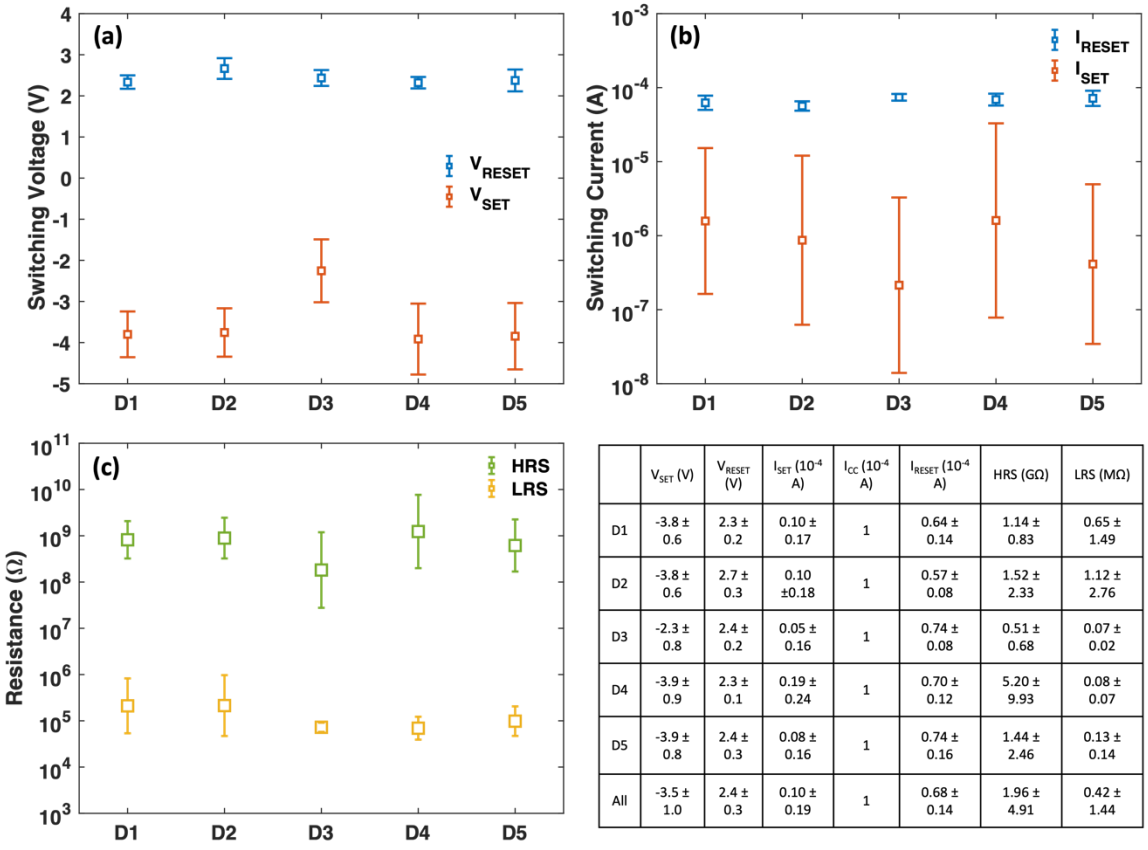
Except the first resistance switching from HRS to LRS is called forming, other following processes of switching the device resistance from HRS to LRS are called SET. In DC mode, the SET process is operated using a dual voltage sweep between 0 and -7 V with a compliance current of 10^{-4} A. Five different devices are tested under DC mode using voltage sweeps, and each device is switched for 20 cycles after the forming process (Figure 2c), exhibiting comparable behavior and low device-to-device variability. The detailed switching parameters are provided in Figure S2, including the SET/RESET voltages and the LRS/HRS resistance distributions. The LRS and HRS are all read at 0.1 V. The retention time of high resistive state (HRS) and low resistive state (LRS) are read at 0.1 V at room temperature. Both resistance states remain stable for 10^4 s without degradation (Figure S3a). As the SET (and forming) processes occur at the compliance current, the LRS remains consistent between devices (Fig. 1c), despite the stochastic nature of the filamentary process.

In pulse mode, the SET process is completed by applying negative voltage pulses with 100 μs pulse width. The height of the voltage pulse increases from -3.5 V to -9.5 V with a step size of 0.5 V until the device is switched back to LRS (Figure S4).

The opposite process of witching the device resistance from LRS back to HRS by partial rupturing of the CFs is called RESET. In DC mode, the RESET process uses a dual voltage sweep between 0 V and 3 V after the forming process (red line annotated by ③ and ④ in Figure 2b) or uses a dual voltage sweep between 0 V and 4V after the SET process. In pulse mode, the RESET process uses positive voltage pulses with 100 μs width. A similar operate-and-verify programming scheme [3–6] is used (Figure S5).

A full round of switching the device resistance from HRS to LRS and then back to HRS is called a switching cycle. The blue lines in Figure 2b represent a typical *I-V* curve of the resistive switching cycle after the first forming-and-RESET cycle. Figure S 6 shows a complete cycle of the switching process in pulse mode.

The switching points are the points where the current jumps up or down abruptly, indicating an abrupt change in device resistance. The switching points can be extracted from the DC *I-V* curves, as noted in Figure 2b. The voltages and the currents of the switching points are defined as the switching voltages and the switching currents, respectively. All the resistances are read at a voltage of 0.1 V.



	V_{SET} (V)	V_{RESET} (V)	I_{SET} (10^{-4} A)	I_{CC} (10^{-4} A)	I_{RESET} (10^{-4} A)	HRS (GΩ)	LRS (MΩ)
D1	-3.8 ± 0.6	2.3 ± 0.2	0.10 ± 0.17	1	0.64 ± 0.14	1.14 ± 0.83	0.65 ± 1.49
D2	-3.8 ± 0.6	2.7 ± 0.3	0.10 ±0.18	1	0.57 ± 0.08	1.52 ± 2.33	1.12 ± 2.76
D3	-2.3 ± 0.8	2.4 ± 0.2	0.05 ± 0.16	1	0.74 ± 0.08	0.51 ± 0.68	0.07 ± 0.02
D4	-3.9 ± 0.9	2.3 ± 0.1	0.19 ± 0.24	1	0.70 ± 0.12	5.20 ± 9.93	0.08 ± 0.07
D5	-3.9 ± 0.8	2.4 ± 0.3	0.08 ± 0.16	1	0.74 ± 0.16	1.44 ± 2.46	0.13 ± 0.14
All	-3.5 ± 1.0	2.4 ± 0.3	0.10 ± 0.19	1	0.68 ± 0.14	1.96 ± 4.91	0.42 ± 1.44

Figure S2. Switching parameters of five different Pt/Al_2O_3/TiO_2 devices under DC voltage sweep mode. (a) Error bar graph of the SET and RESET switching voltages, (b) error bar graph of the SET and RESET switching currents, (c) error bar graph of the HRS and LRS. The table on the bottom-right side lists all the parameters in detail.

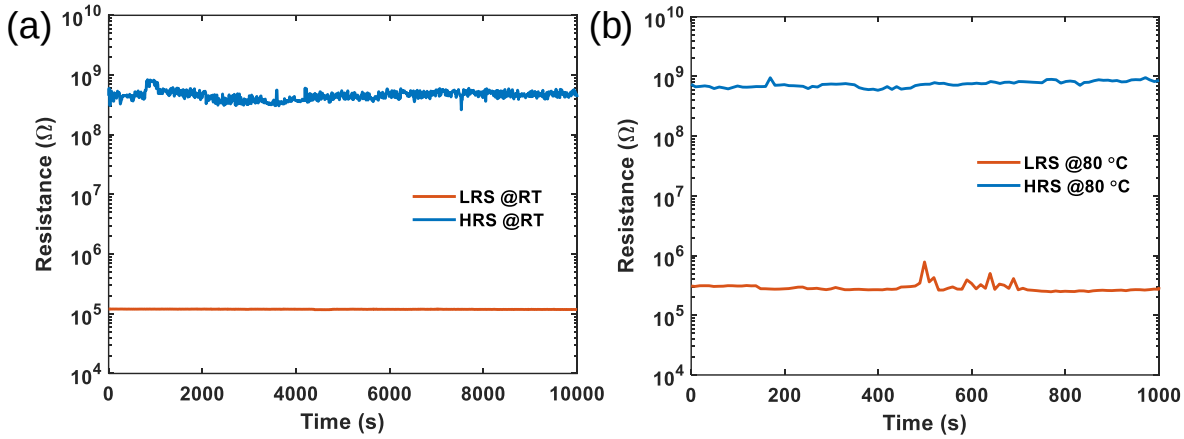


Figure S3. (a) Retention time of HRS and LRS at room temperature. The resistance is read at 0.1 V. The lower noise in the LRS current is the result of the higher currents there relative to the HRS state. (b) The LRS and HRS retention times at 80 °C and 0.1 V.

An operate-and-verify programming scheme is used here, which means more than a single pulse may be used in the SET or RESET operations. The voltage height in both SET and RESET process will increase until the resistance is tuned to the destination resistance value. The details of the operate-and-verify programming scheme is shown in Figure S4-S6. The reason for using the operate-and-verify programming scheme is that the device might not reach the desired resistance range after a single pulse operation. To ensure the device's resistance is indeed programmed to the desired value, the verification step is necessary. This operate-and-verify programming scheme requires higher energy consumption compared to single-pulse programming scheme, but is more reliable and guarantees the resistance modulation success for each cycle.

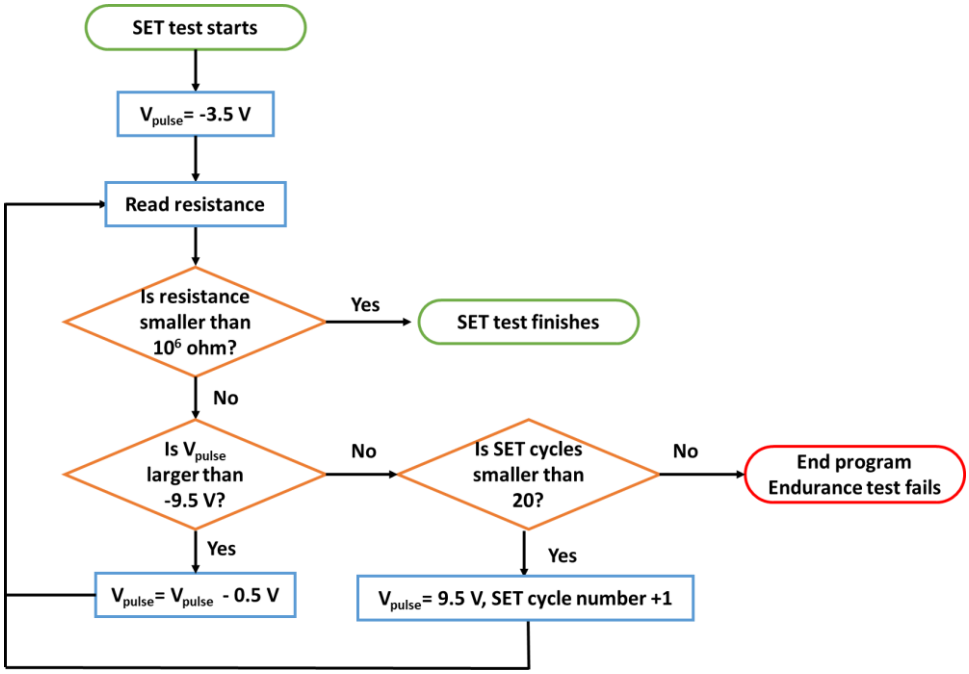


Figure S4. Chart flow of the SET process under pulse mode.

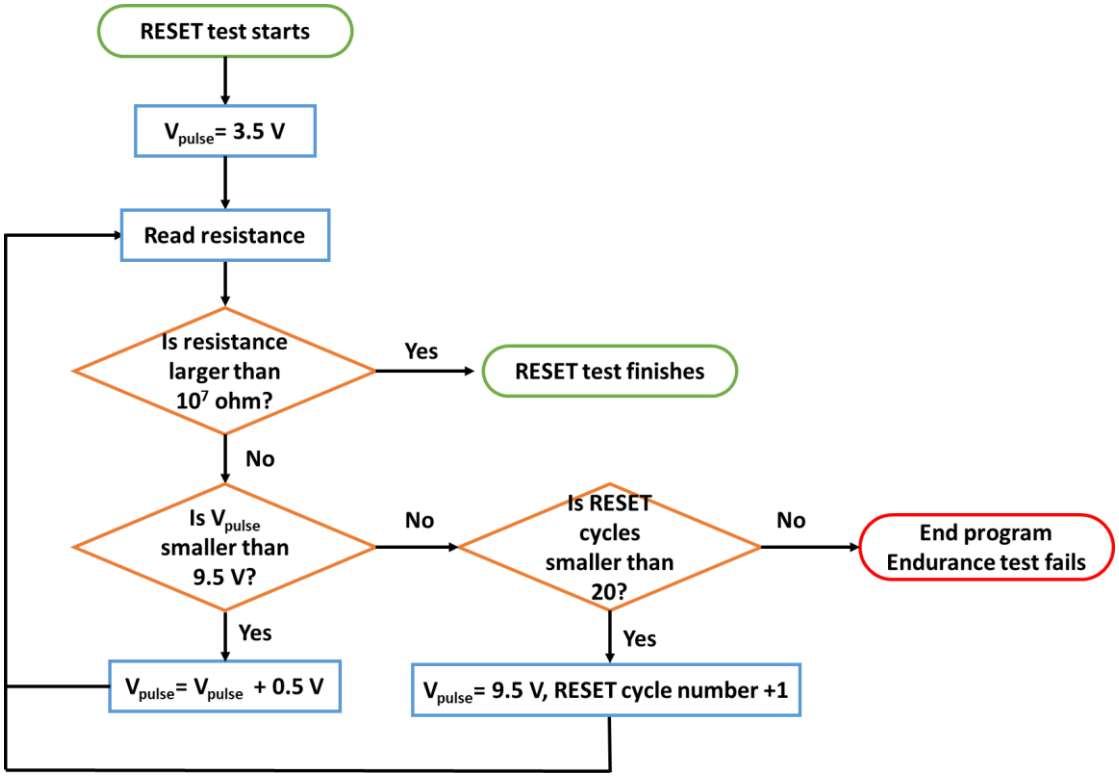


Figure S5. Chart flow of the RESET process under pulse mode.

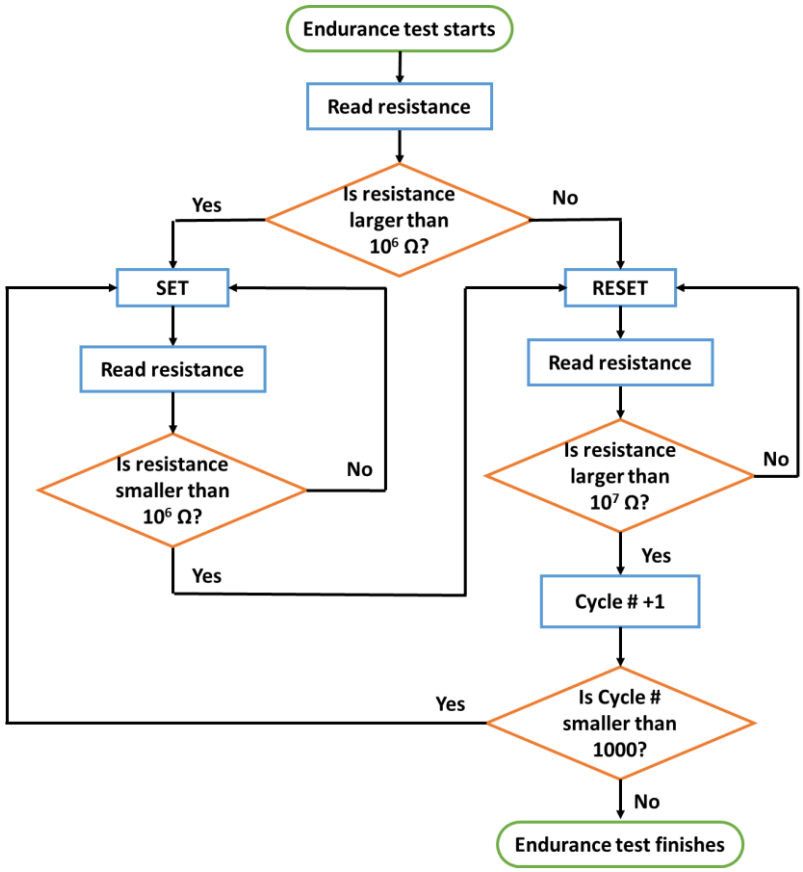


Figure S6. Chart flow of the endurance test under pulse mode.

Supplementary Information References

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